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MS-7760 Ver: 2.0

CPU:

INTEL - Sandy Bridge-E LGA2011

System Chipset:

INTEL - Patsburg PCH

OnBoard Chipset:

Clock Gen:932SQ420D + 9FG1200AG-5LF

LAN:Intel PHY82579

USB3.0: UPD720200F1 X2

Flash ROM: 8 MB SPI / 8 MB SPI (PCH)

SIO:FIN71889AD(LAA)

Main Memory:

DDRIII (1066/1333MHz) * 8

PWM:

CPU:uP1618 (8-Dr.MOS)

CPU_SA:uP1618 (1-Dr.MOS)

CPU_VTT:UP6212 (2-Dr.MOS)

VCC_DDR:UP6212(2-Dr.MOS)

PCH:uP1508 (1-Dr.MOS)

ACPI:

UPI

Other:

SATA3.0 *2+SATA2.0 *4

USB2.0 *14 (Rear*6 Front*8)

Expansion Slots:

PCI Express (X16) Slot * 2

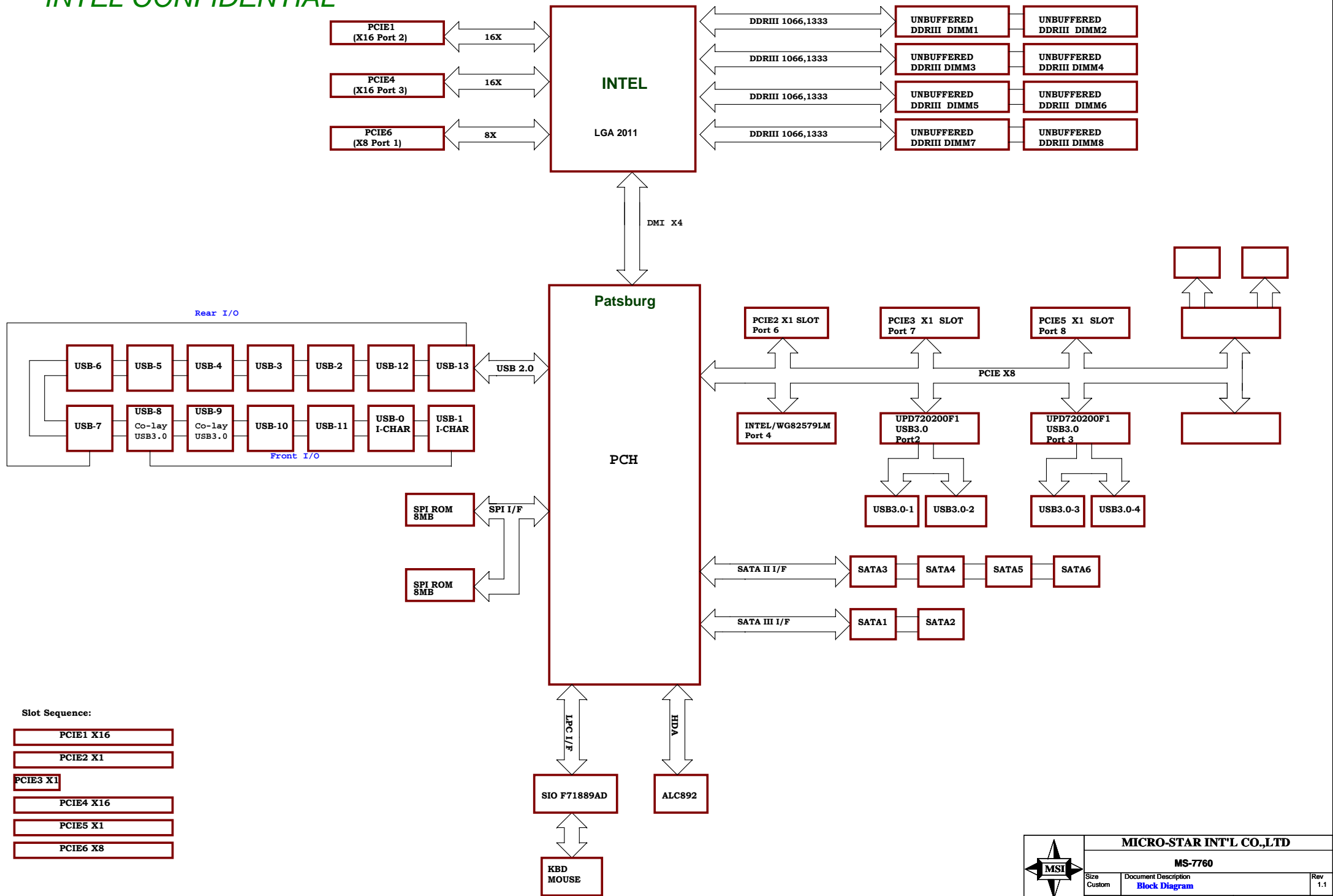
PCI Express (X8) Slot * 1

PCI Express (X1) Slot * 3

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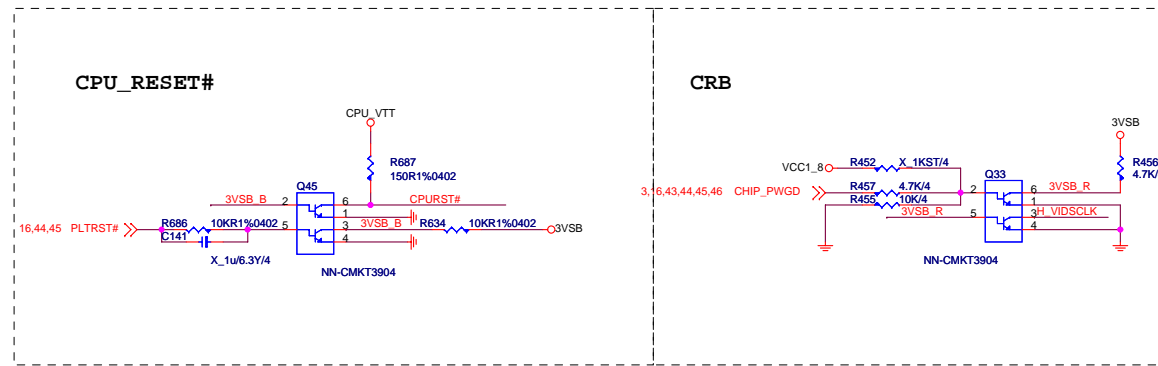
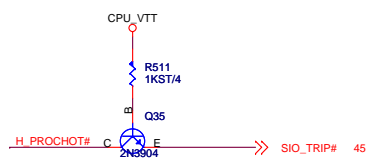
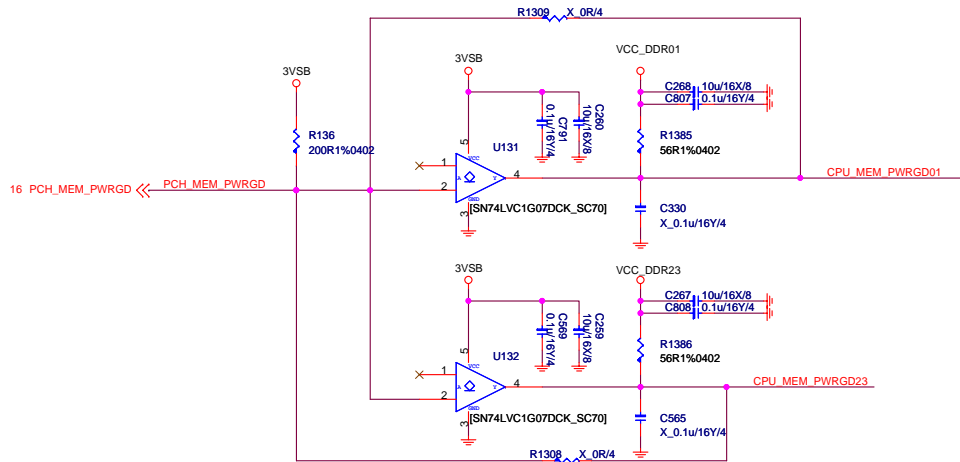
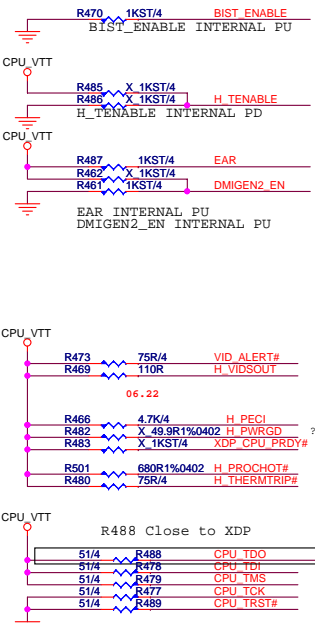
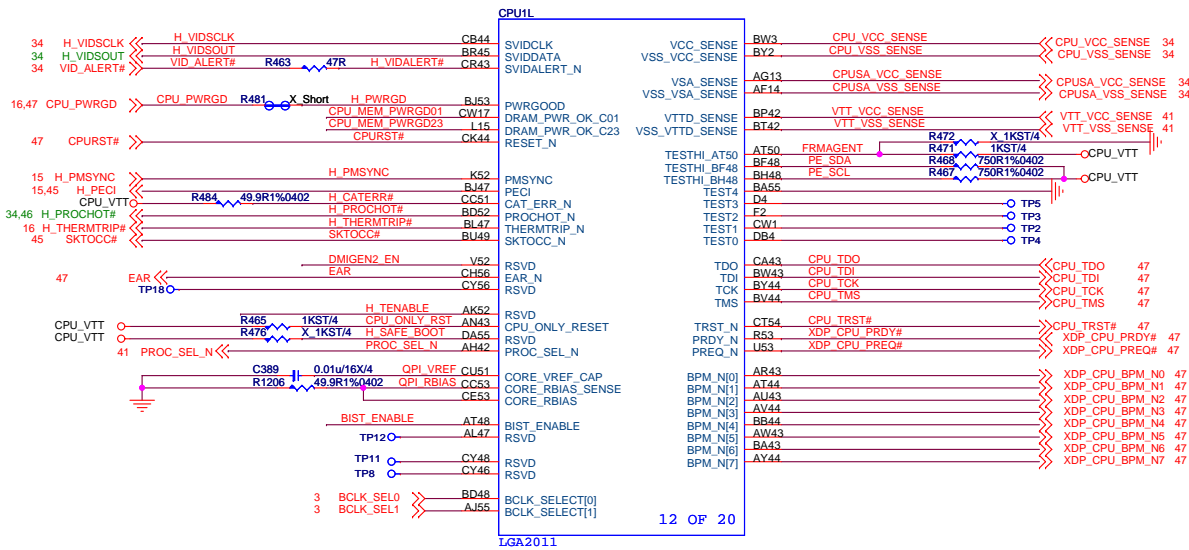
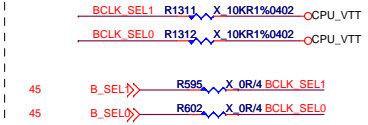


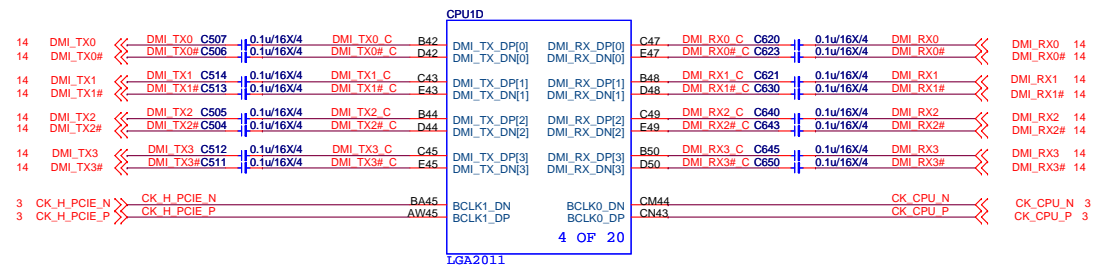
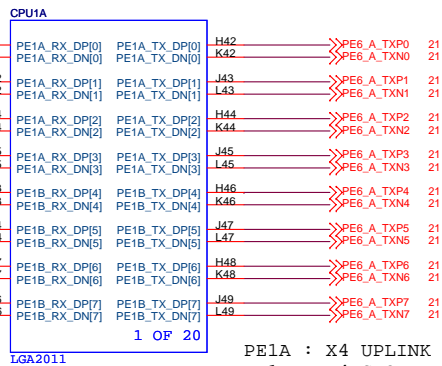
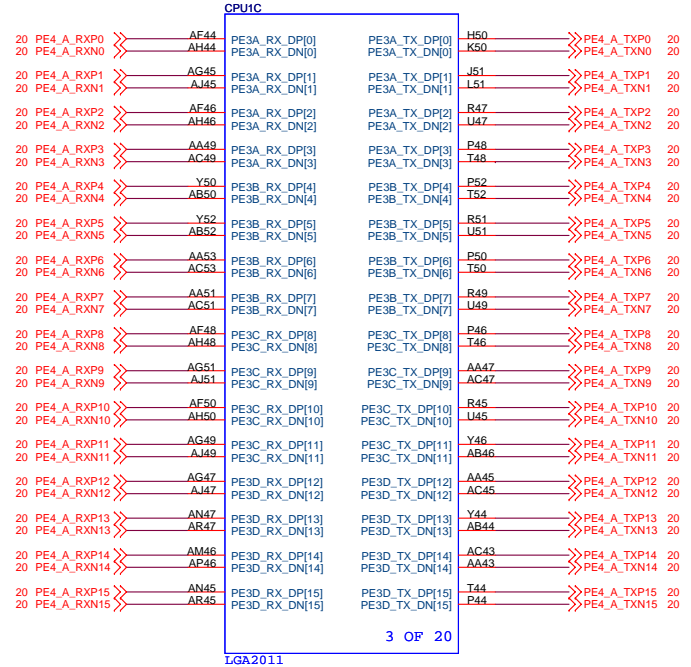
MICRO-STAR INT'L CO.,LTD		
MS-7760		
Size Custom	Document Description Cover Sheet	Rev 1.1
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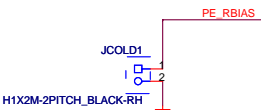
BLCK SELECT

BCLK_SEL1	BCLK_SEL0	BCLK Selected
X	X	100MHz (default)
1	1	100MHz
1	0	125MHz
0	1	167MHz (RSVD)
0	0	250MHz (RSVD)





Reserve for Cold Bug

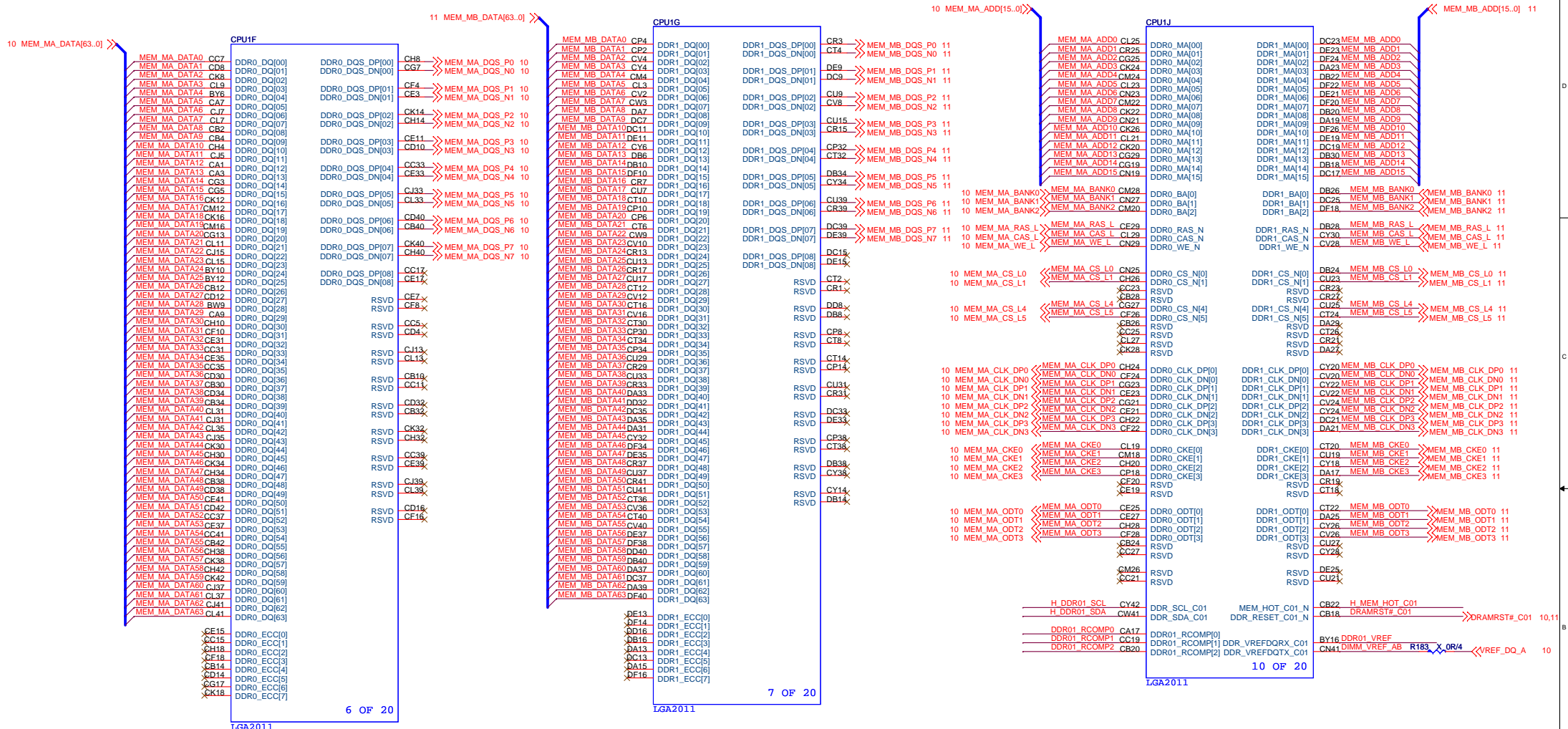


MICRO-STAR INT'L CO.,LTD

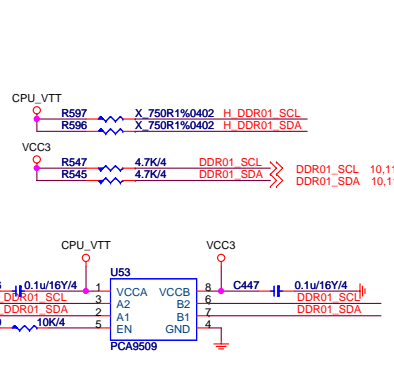
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Size Custom Document Description CPU-PEG/DMI Rev 1.1

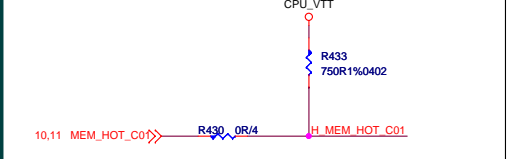
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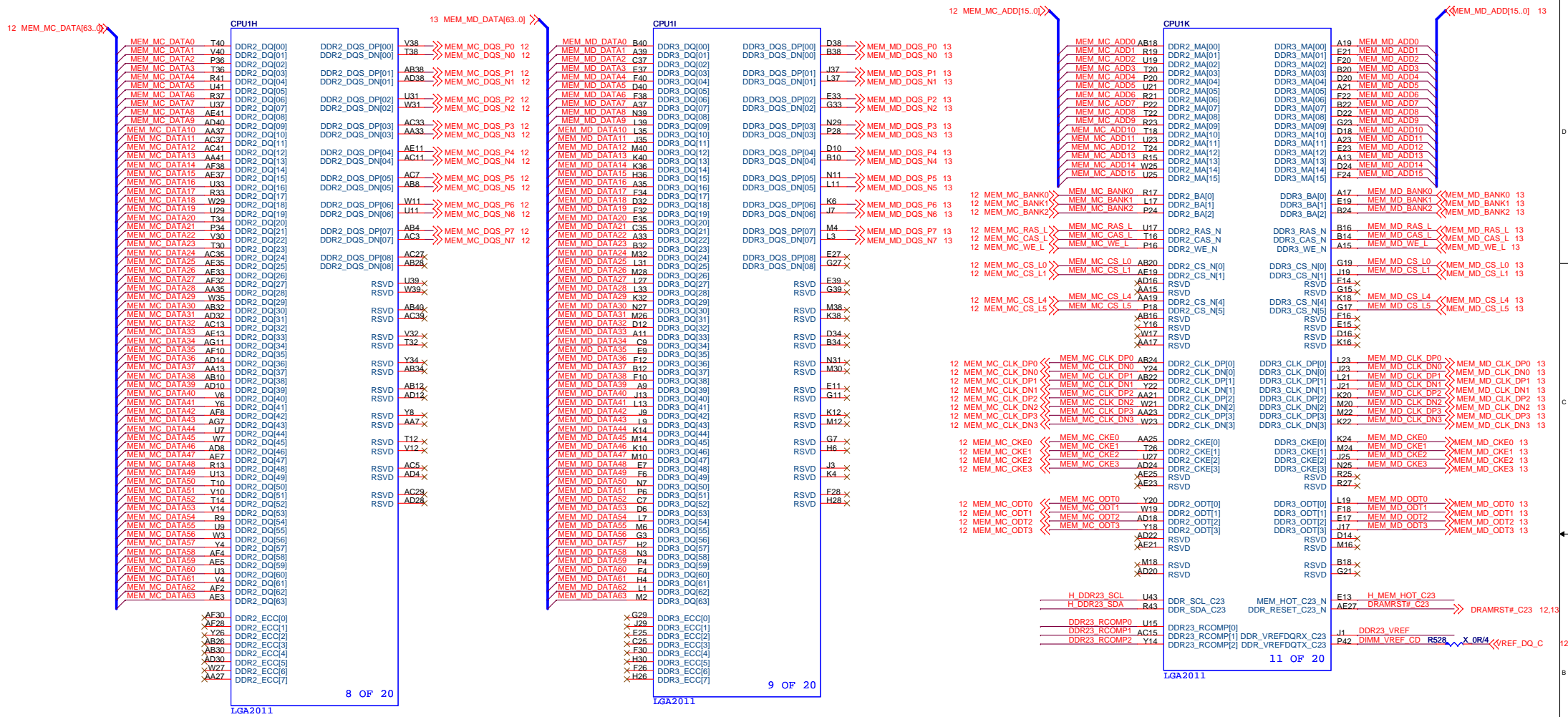
Level Shift



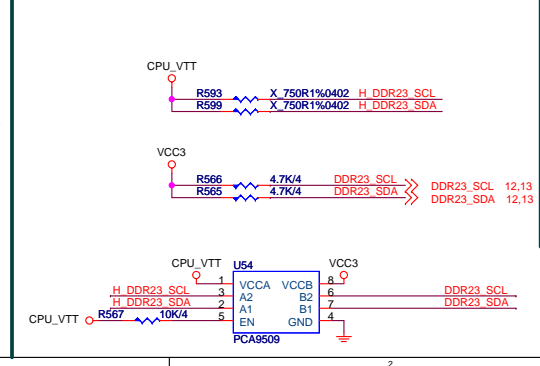
Memory Hot



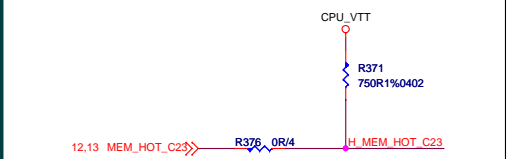
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Level Shift



Memory Hot

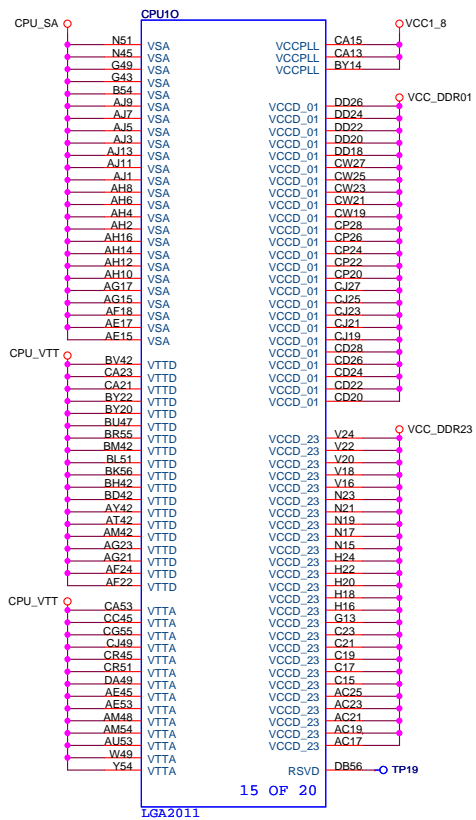
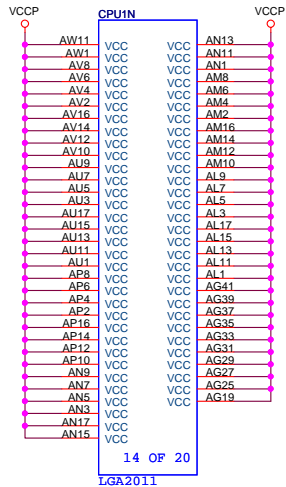
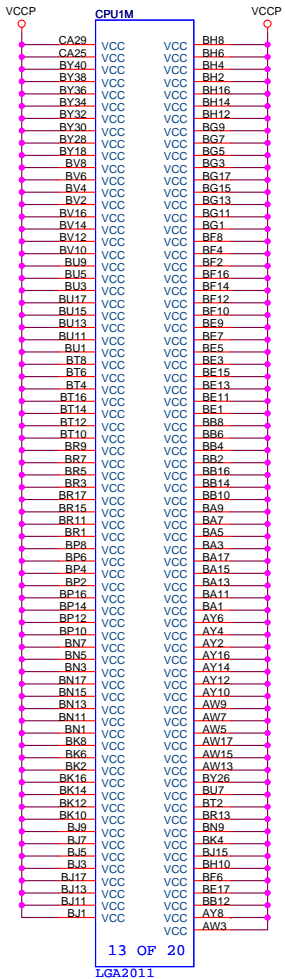


MICRO-STAR INT'L CO.,LTD

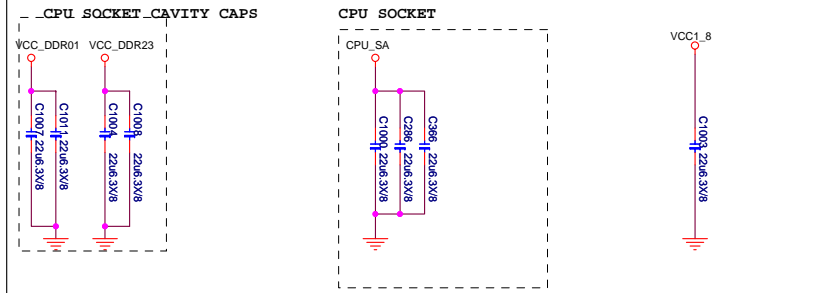
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Size: Custom | Document Description: CPU-Memory 2&3 | Rev: 1.1

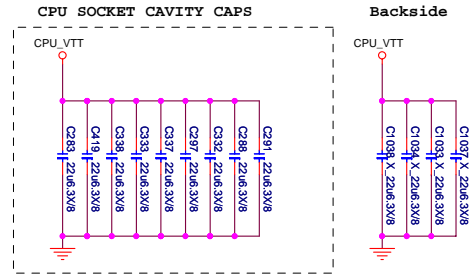
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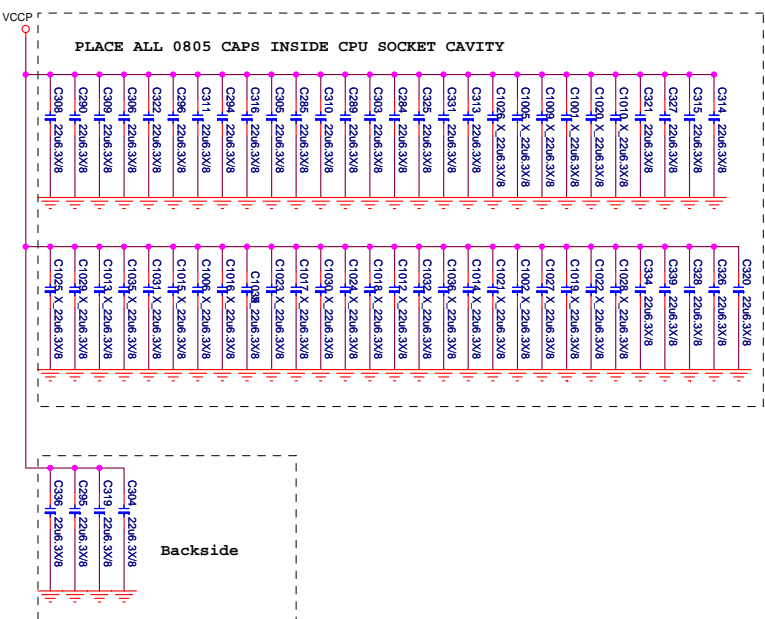
+1.5V_DDR3-Decoupling **+CPU_SA Decoupling** **+VCC1_8 Decoupling**

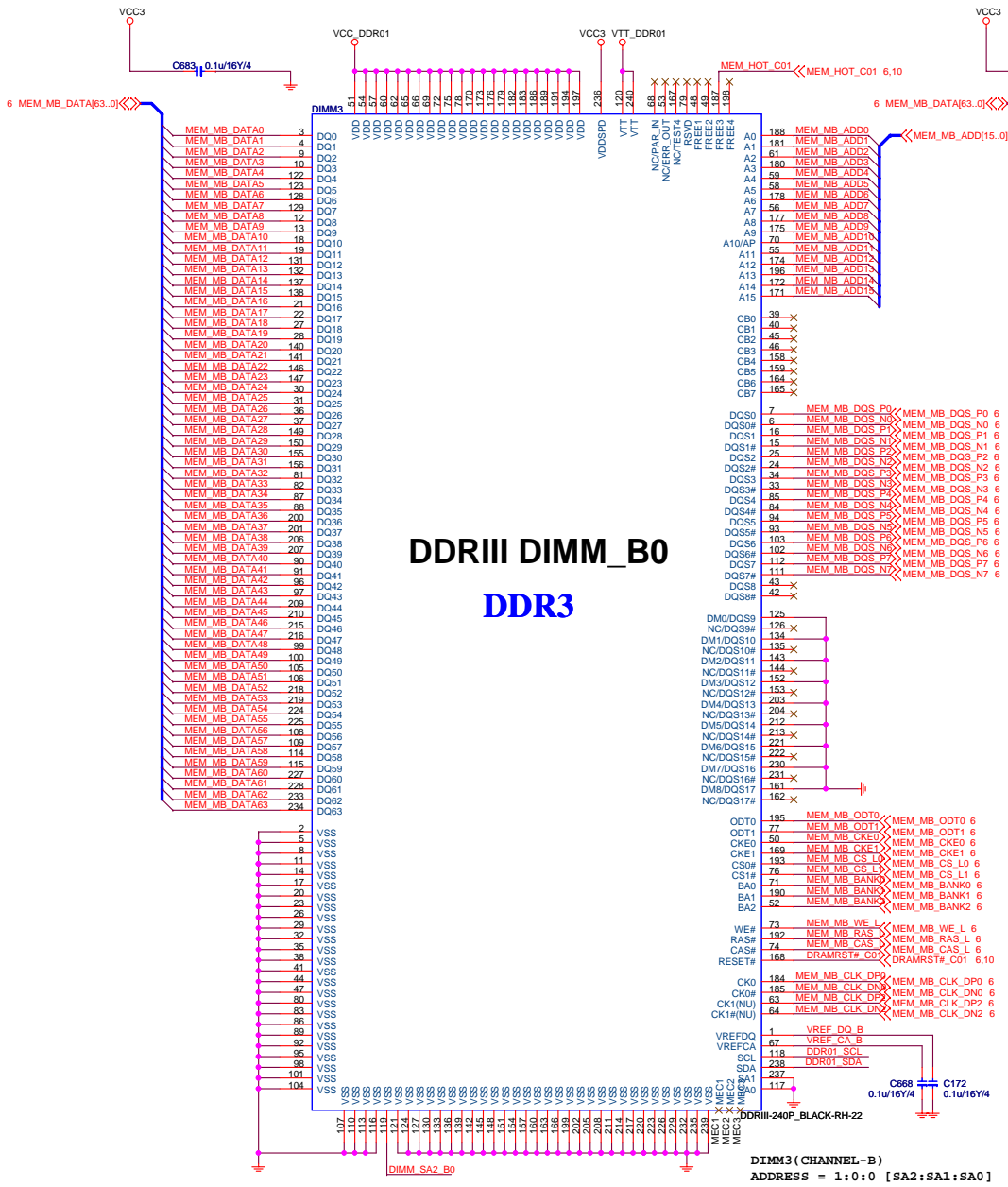


+CPU_VTT Decoupling



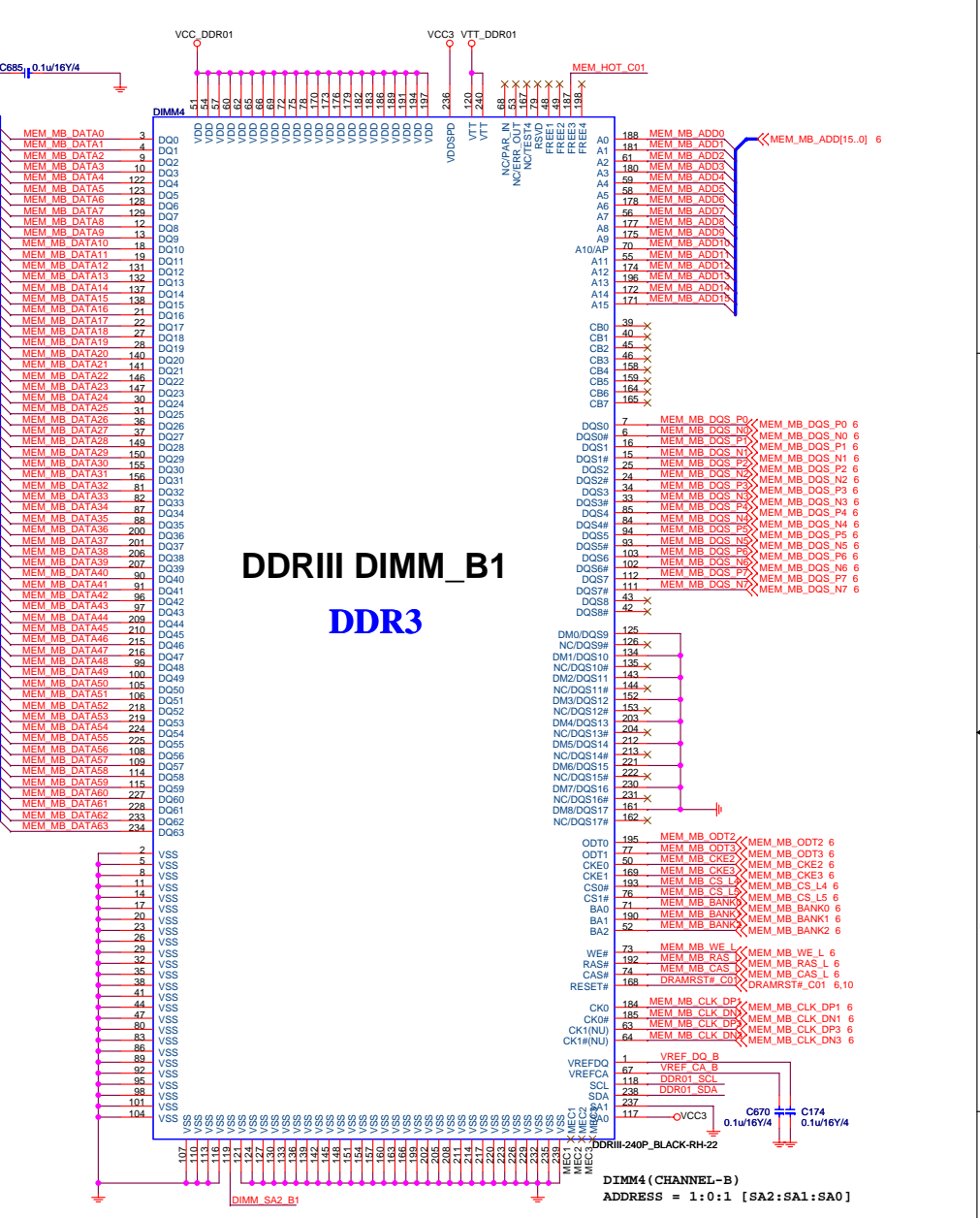
+CPU_VCCP-Decoupling





DDR3 DIMM_B0

DDR3



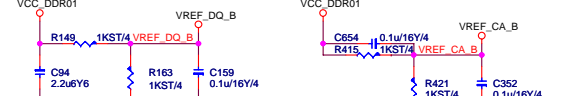
DDR3 DIMM_B1

DDR3

Warning LED



Close DIMM3

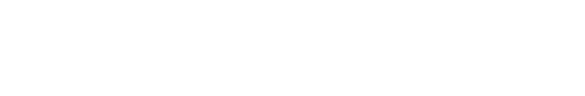


VREF_DO_B VREF_DO_B 10

Warning LED

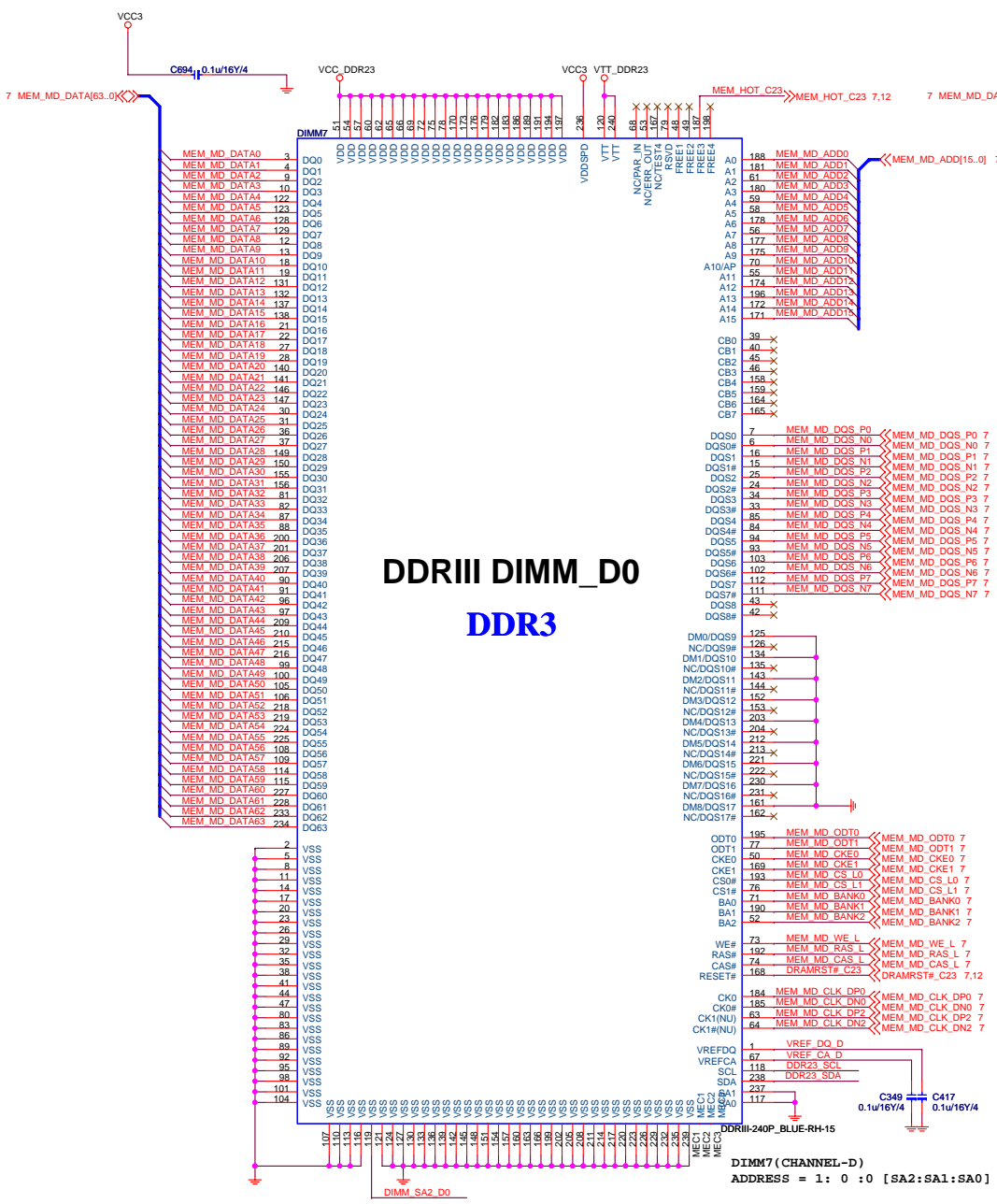


Close DIMM4

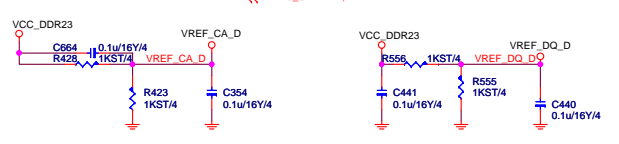
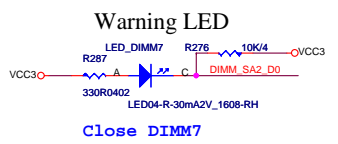


VREF_DO_B VREF_DO_B 10

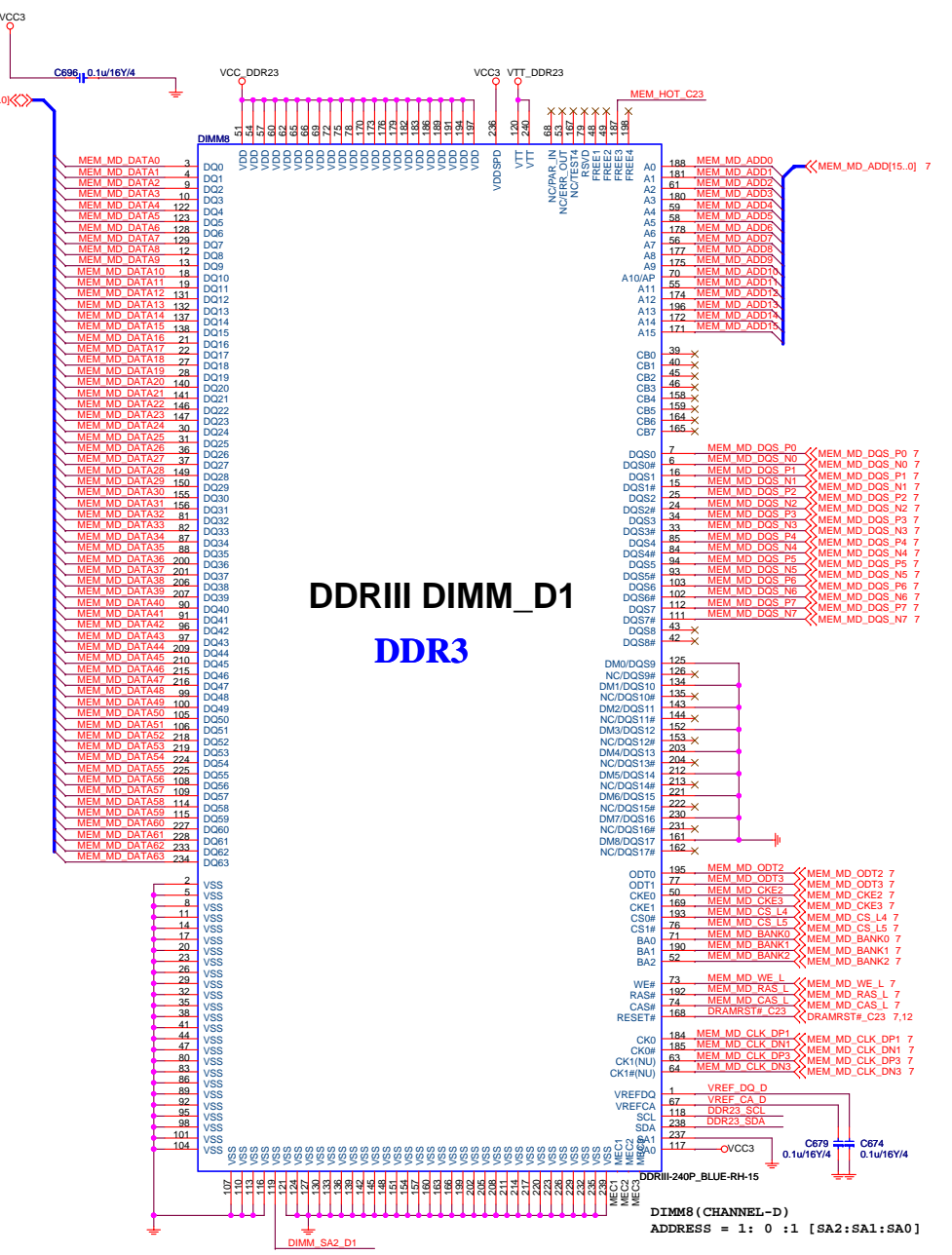
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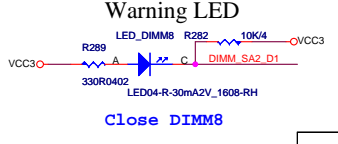
DDR3 DIMM_D0
DDR3



VREF_DQ_D VREF_DQ_D 12



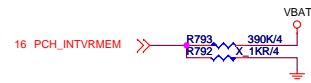
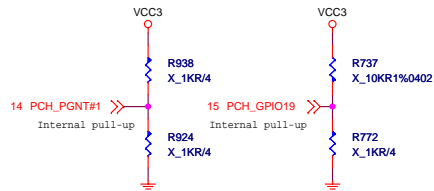
DDR3 DIMM_D1
DDR3



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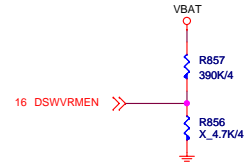
PCH Straps

BOOT DEVICE	GNT1	SATA1GP/GPIO19
LPC	0	0
PCI	1	0
SPI	1	1



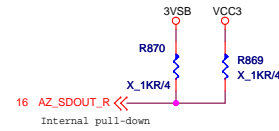
INTRVMEM
 0 : DISABLE INTERNAL VRM
 1 : ENABLE INTERNAL VRM *

When these voltage regulators are enabled, the integrated GbE only operates at 10/100 Mbps during S3-S5.

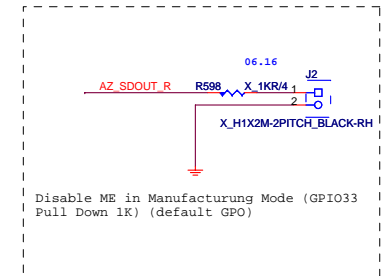


DSWVRMEN
 0 : Disable Internal Deep Sleep 1.05 V regulators.
 1 : Enable Internal Deep Sleep 1.05 V regulators.

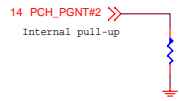
This signal enables the internal Deep Sleep 1.05 V regulators. Must be connected even when not supporting DSW.



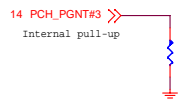
HDA_SDO
 Disable ME in Manufacturing Mode when pull LOW ????



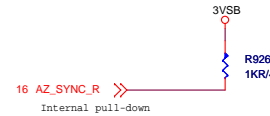
Disable ME in Manufacturing Mode (GPIO33 Pull Down 1K) (default GPO)



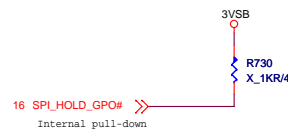
DMI AC/DC MODE
 0 : AC*
 1 : DC



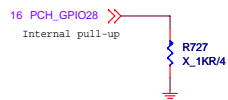
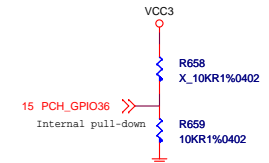
Topblock swap override when pull-low
 Signal has a weak internal pull-up



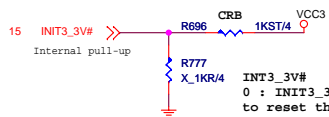
HDA_SYNC
 OD PLL VR SUPPLY SEL
 0 : 1.8V SUPPLY
 1 : 1.5V SUPPLY *



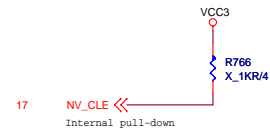
GPIO15
 0 : TLS CIPHER SUITE WITH NO CONFIDENTIALITY *
 1 : TLS CIPHER SUITE WITH CONFIDENTIALITY



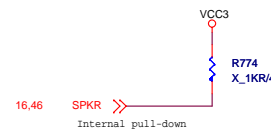
GPIO28
 0 : OD PLL VR disabled
 1 : OD PLL VR enabled *
 Signal has a weak internal pull-up



INT3_3V#
 0 : INIT3_3V to asserted for 16 PCI clock to reset the processor by some evens occur
 1 : Can not to reset the processor



DMI/FDI TERMINATION VOLTAGE
 DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH
 DC COUPLED: TX/RX TO VSS IF SAMPLED LOW *?
 AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP

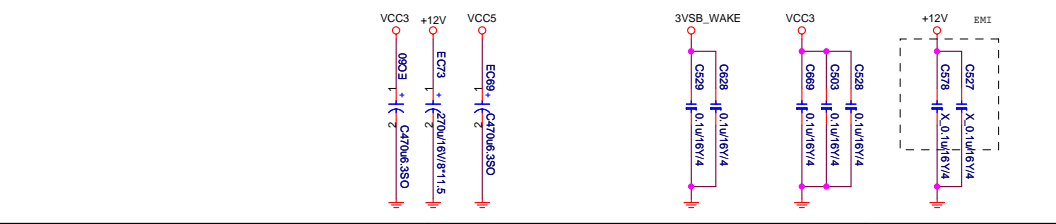
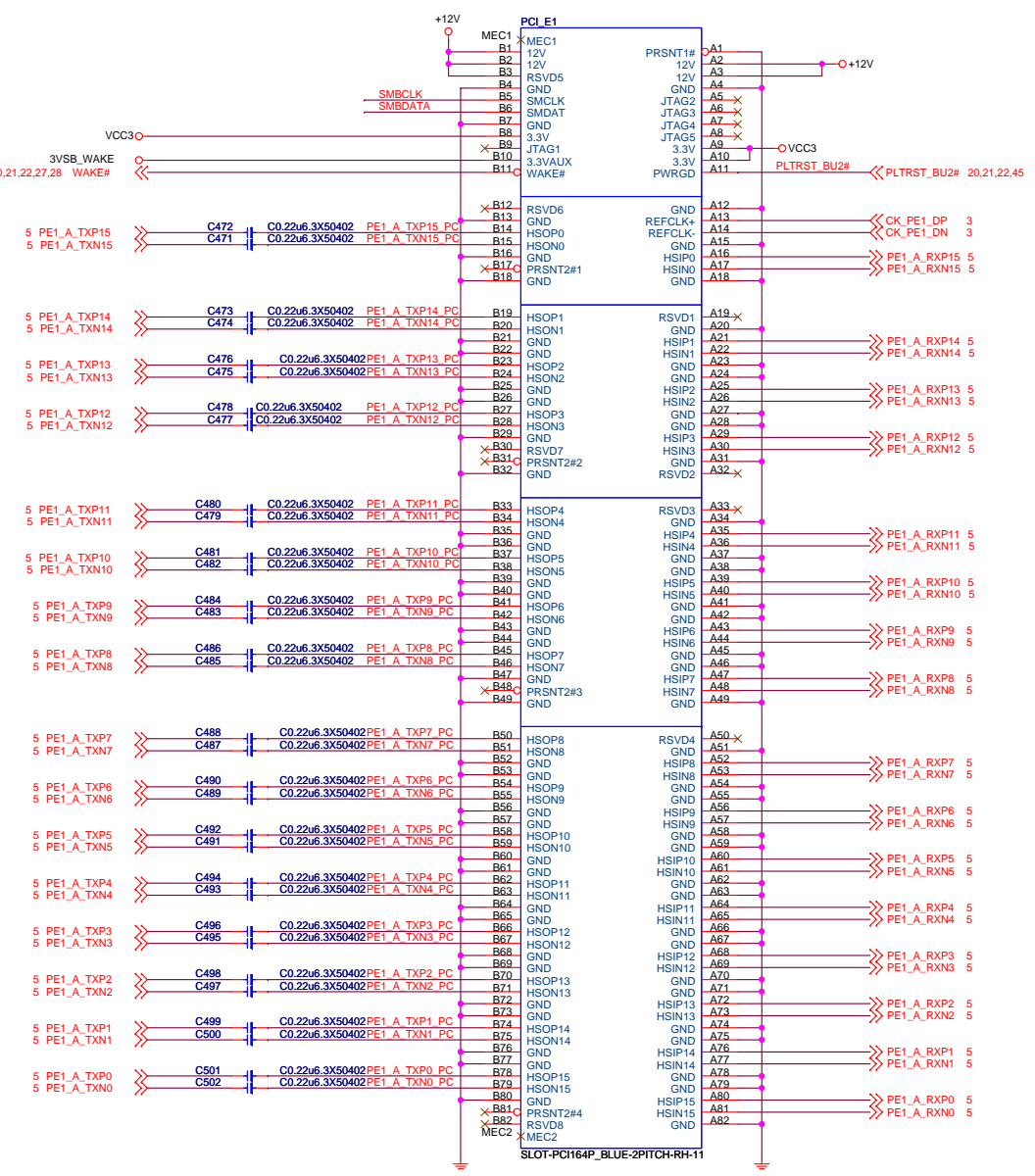


SPKR
 0 : EN TCO REBOOT *
 1 : DIS TCO REBOOT

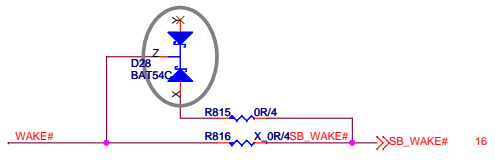
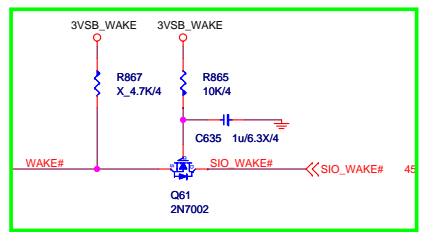


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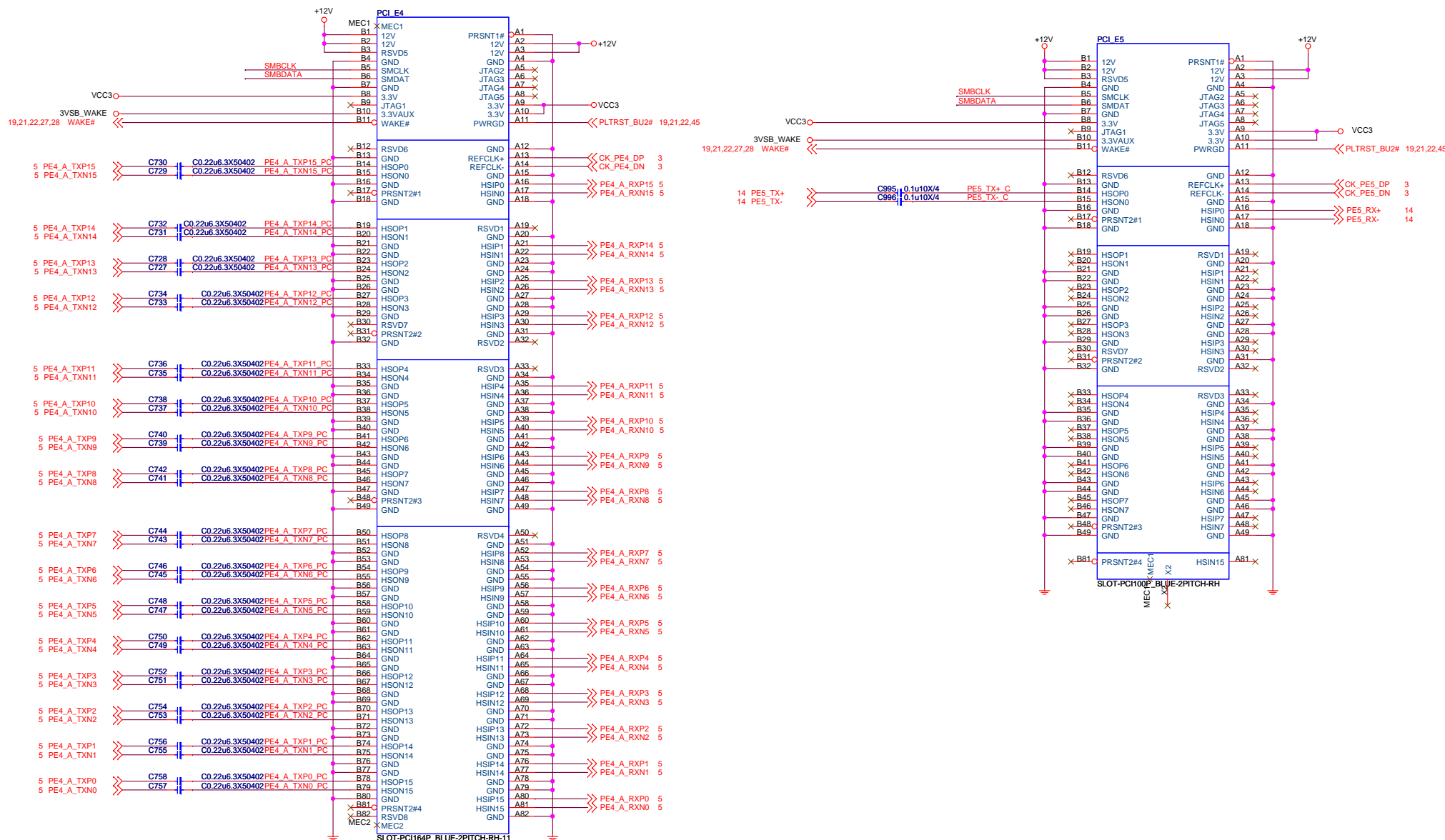


PCIE Wake Up CTRL Circuit

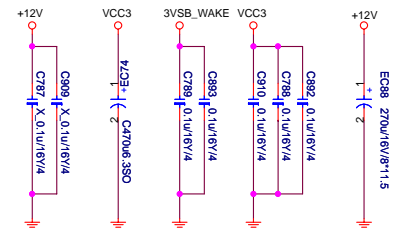


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MS-7760		
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3,10,12,16,19,21,22,23,32,34,43,44,46,47 SMBCLK
 3,10,12,16,19,21,22,23,32,34,43,44,46,47 SMBDATA



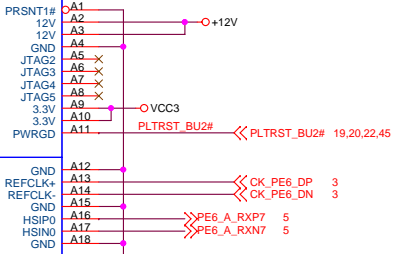
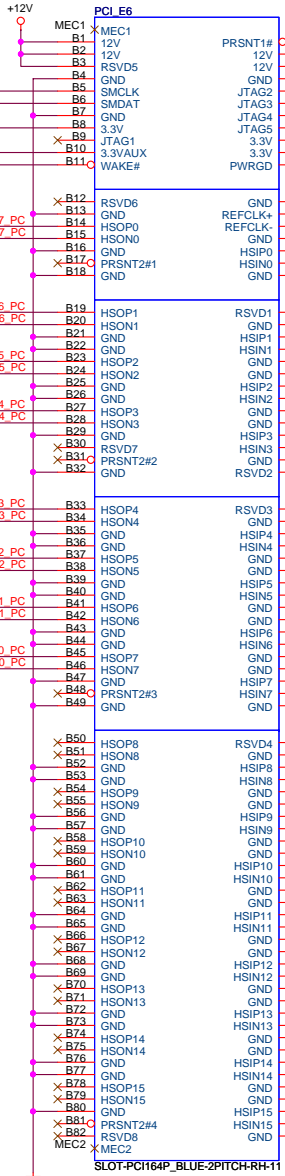
within 500mil



MSI			MICRO-STAR INT'L CO.,LTD		
			MS-7760		
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3,10,12,16,19,20,22,23,32,34,43,44,46,47
 3,10,12,16,19,20,22,23,32,34,43,44,46,47

SMBCLK
 SMBDATA



3VSB_WAKE
 WAKE#

PE6_A_TXP7
 PE6_A_TXN7

PE6_A_TXP6
 PE6_A_TXN6

PE6_A_TXP5
 PE6_A_TXN5

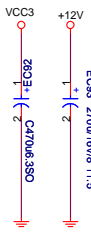
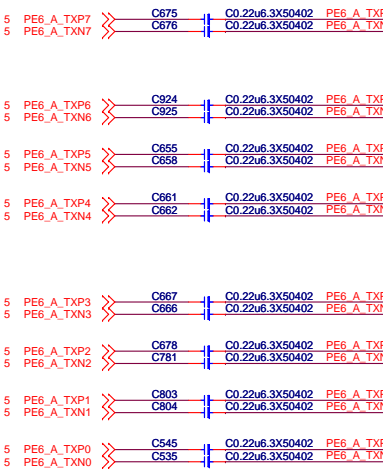
PE6_A_TXP4
 PE6_A_TXN4

PE6_A_TXP3
 PE6_A_TXN3

PE6_A_TXP2
 PE6_A_TXN2

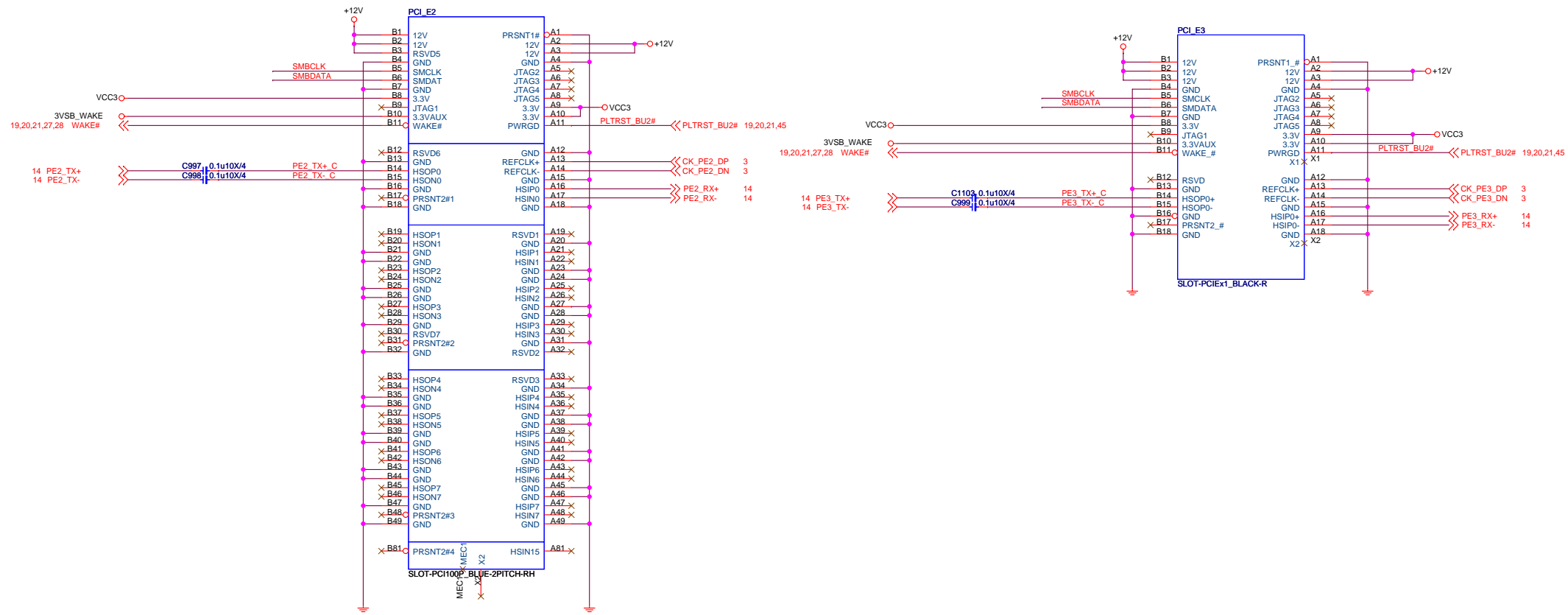
PE6_A_TXP1
 PE6_A_TXN1

PE6_A_TXP0
 PE6_A_TXN0




SLOT-PCI164P_BLUE-2PITCH-RH-11

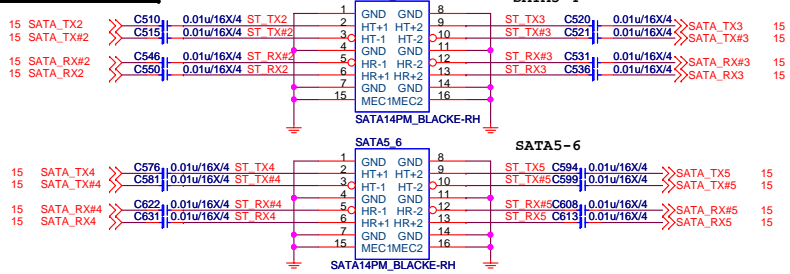
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MICRO-STAR INT'L CO.,LTD		
MS-7760		
Size Custom	Document Description PCI-E X8 & Switch	Rev 1.1
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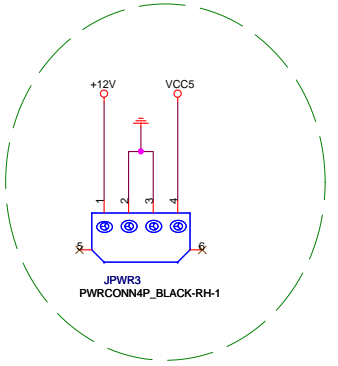
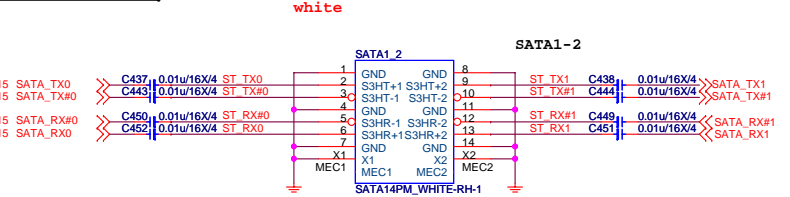
3,10,12,16,19,20,21,23,32,34,43,44,46,47 SMBCLK <> SMBCLK
 3,10,12,16,19,20,21,23,32,34,43,44,46,47 SMBDATA <> SMBDATA

			MICRO-STAR INT'L CO.,LTD		
MS-7760			MSI		
Size	Document Description				Rev
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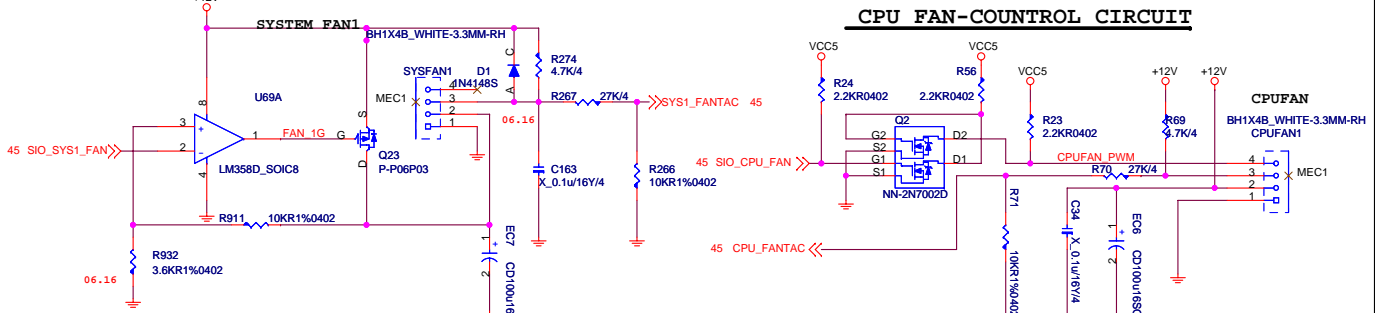
SATA2 Ports



SATA3 Ports



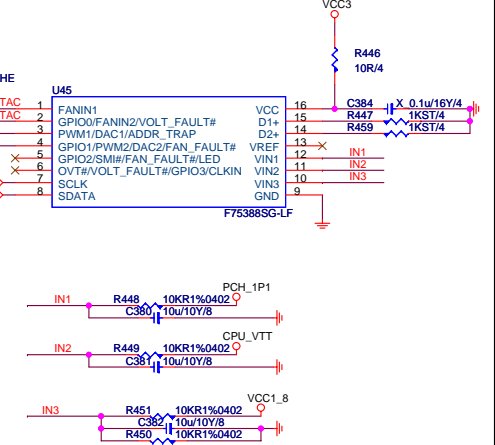
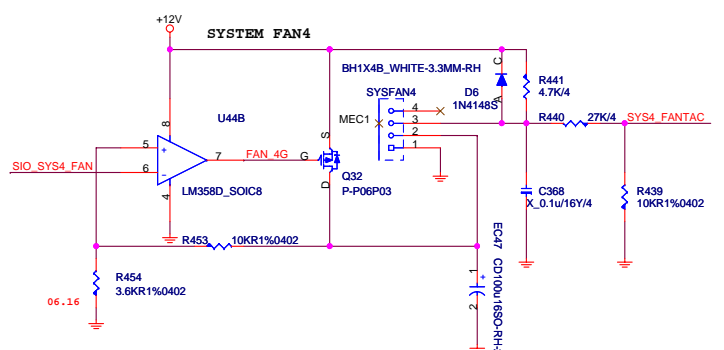
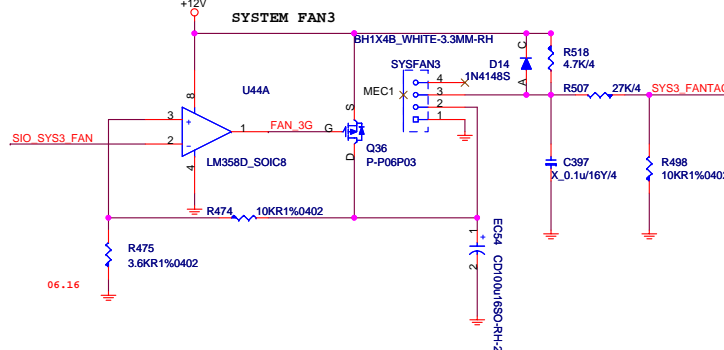
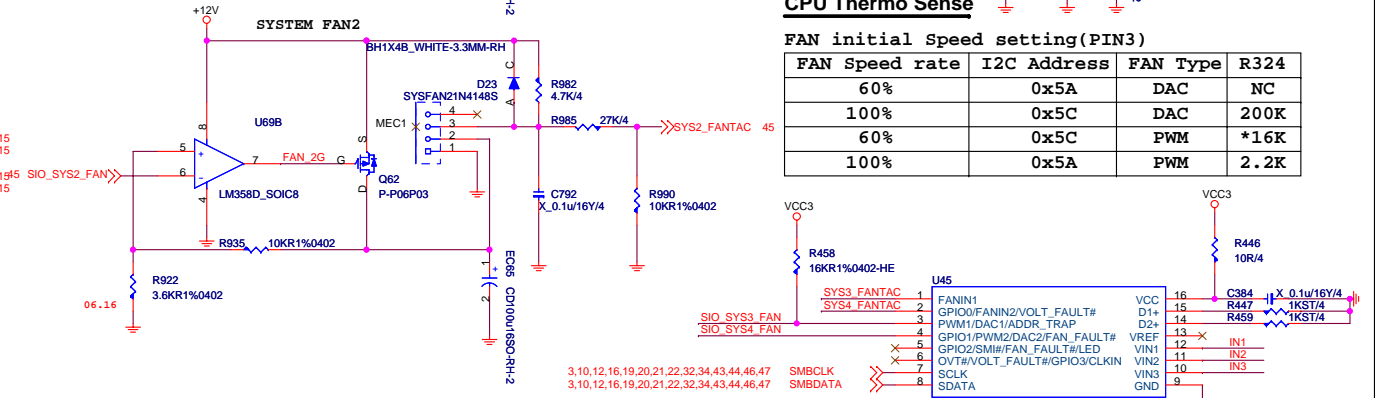
CPU FAN-COUNTROL CIRCUIT



CPU Thermo Sense

FAN initial Speed setting(PIN3)

FAN Speed rate	I2C Address	FAN Type	R324
60%	0x5A	DAC	NC
100%	0x5C	DAC	200K
60%	0x5C	PWM	*16K
100%	0x5A	PWM	2.2K



HW Monitor

MICRO-STAR INT'L CO.,LTD

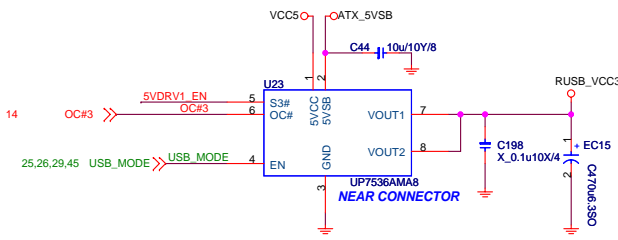
MS-7760

Size	Document Description	Rev
Custom	SATA/SAS Ports and Fan Control	1.1

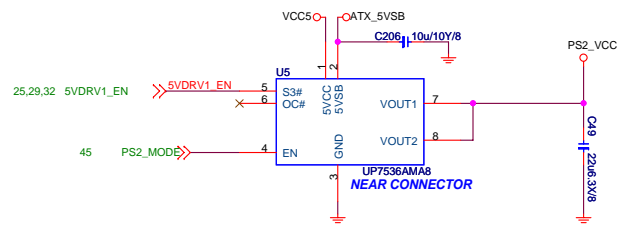
Date: Wednesday, October 12, 2011 | Sheet 23 of 54

Rear USB Connector

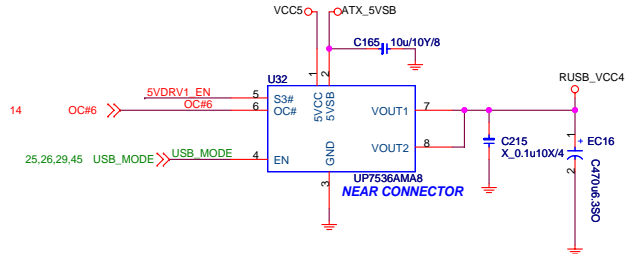
USB POWER FOR PORT 6,7



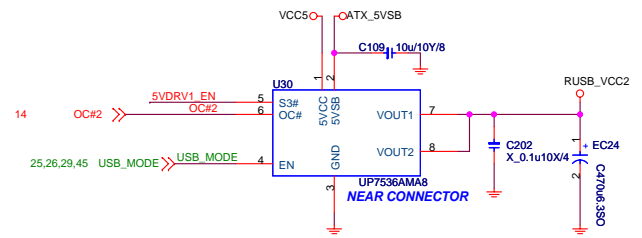
PS2 POWER



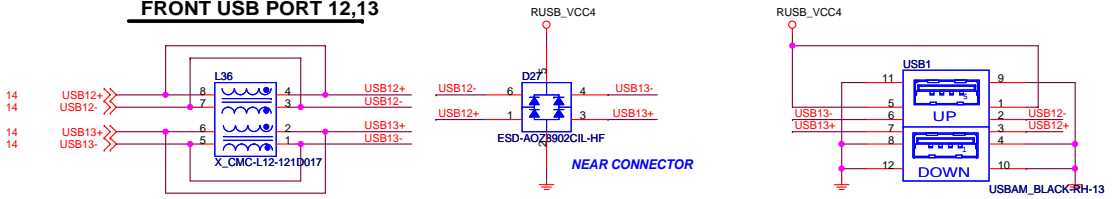
USB POWER FOR PORT 12,13



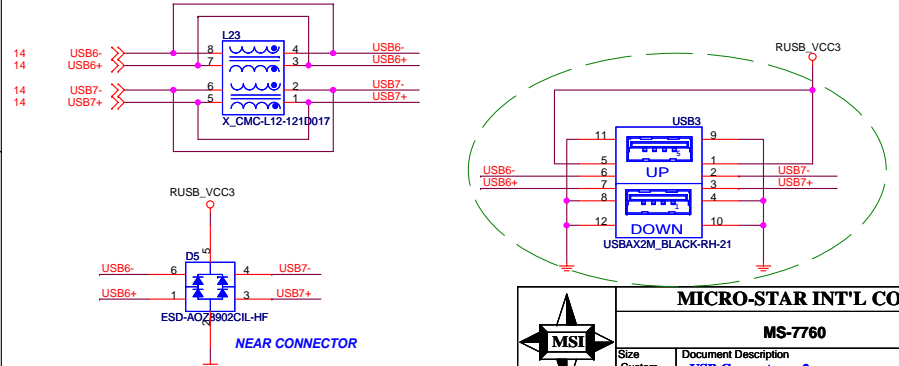
USB POWER FOR PORT 4,5



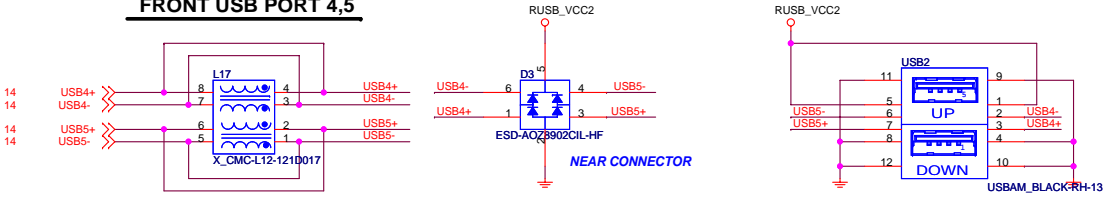
FRONT USB PORT 12,13



FRONT USB PORT 6,7



FRONT USB PORT 4,5

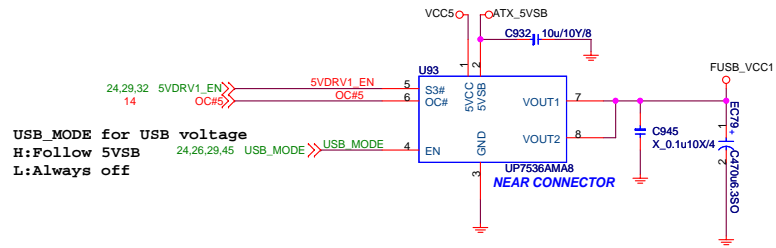


MICRO-STAR INT'L CO.,LTD

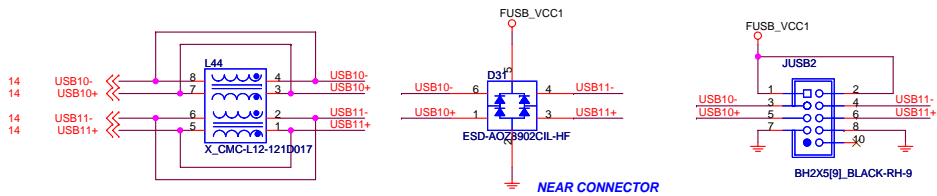
MS-7760

Size	Document Description	Rev
Custom	USB Connectors - 2	1.1
Date: Wednesday, October 12, 2011	Sheet 24	of 54

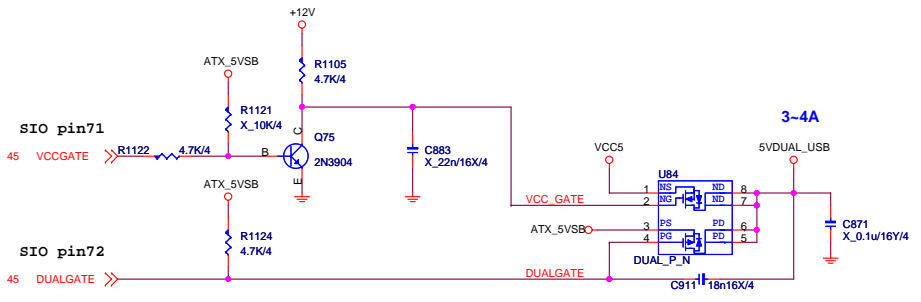
USB POWER FOR 10,11



FRONT USB PORT 10,11



5VDUAL_USB



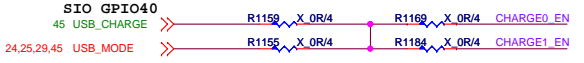
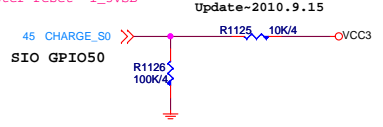
SIO GPIO40 Pin7 (I_VSB3V)

USB_CHARGE: (OD)
 0: Don't support USB charge and resume.
 1: Support USB charge and resume.

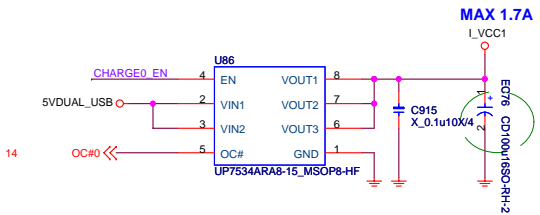
Power plug in , H/W default support USB charge.

Pin power I_3VSB or VBAT
 Register power I_3VSB or VBAT
 Register reset I_3VSB or VBAT

Pin power I_3VSB
 Register power I_3VSB
 Register reset I_3VSB

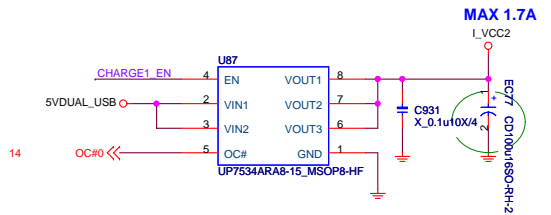


USB POWER PORT 0 For USB Charging

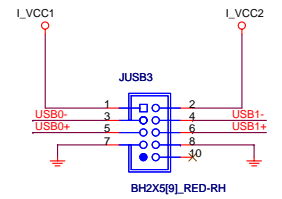
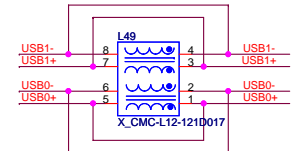


** If your spec will not need bom option, please don't co-lay blue labels.

USB POWER PORT 1 For USB Charging

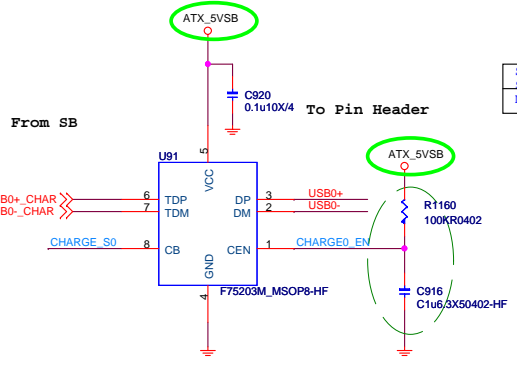


FRONT USB PORT 0,1

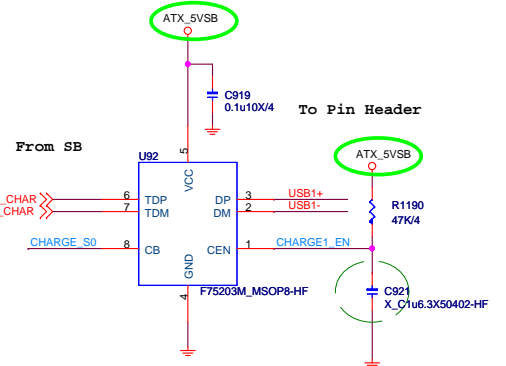


Please name the pin header JUSB1 and use SB USB0,1 link for charger port.

PI5USB14550 has internal EDS diode.



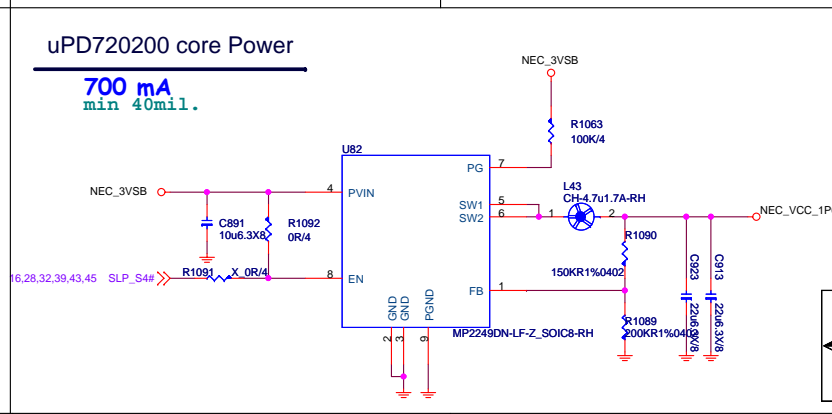
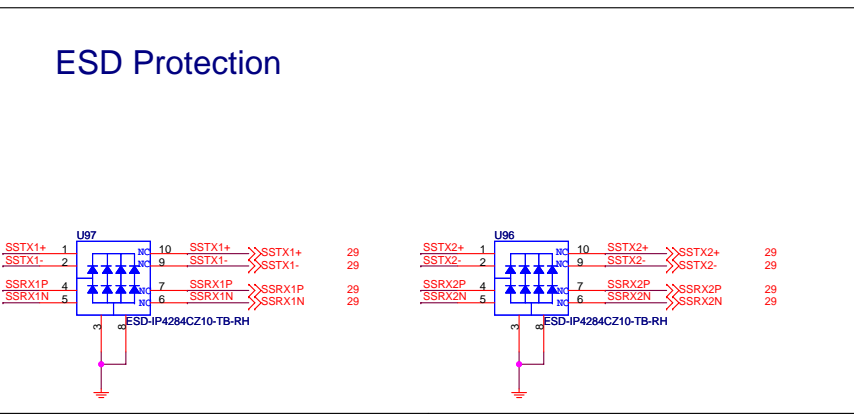
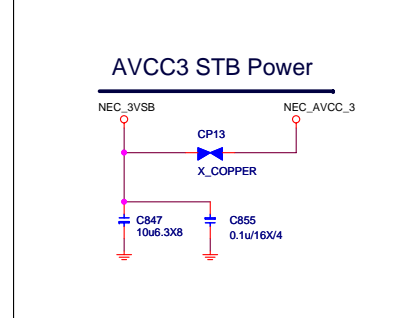
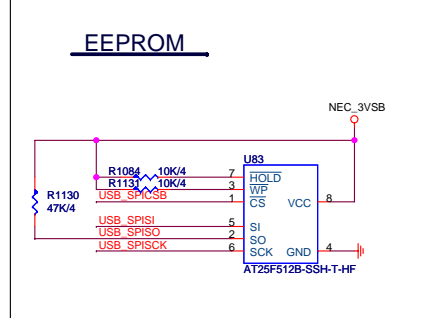
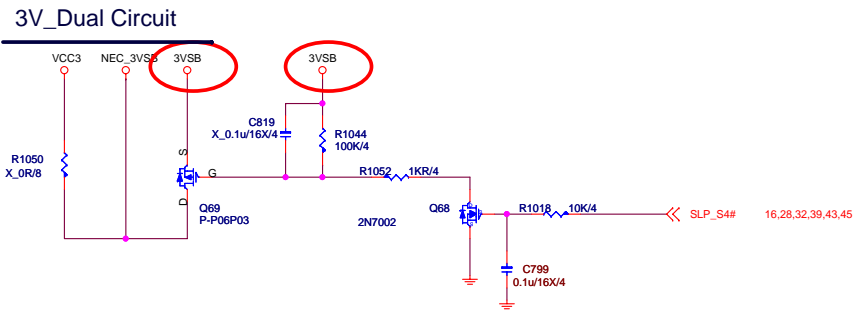
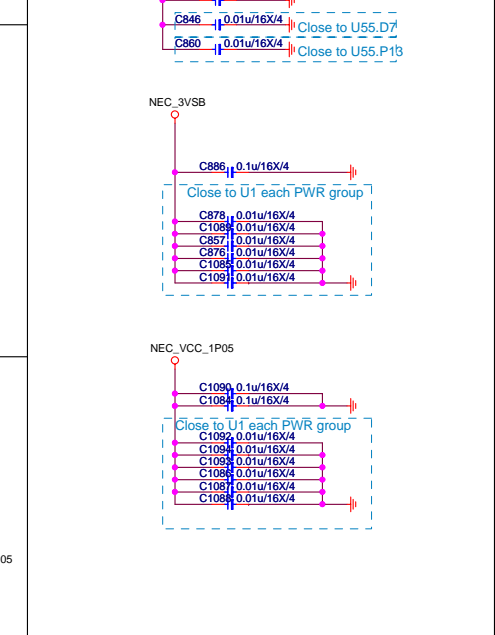
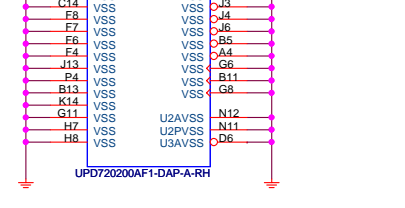
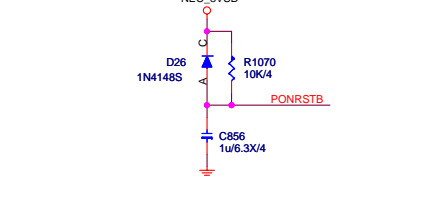
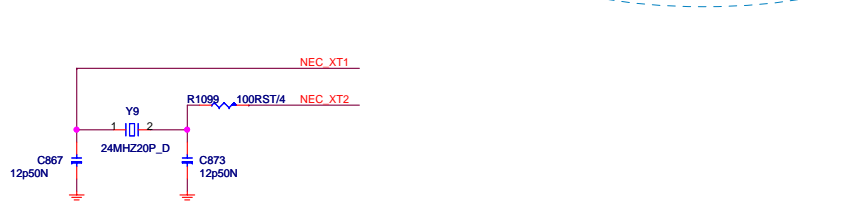
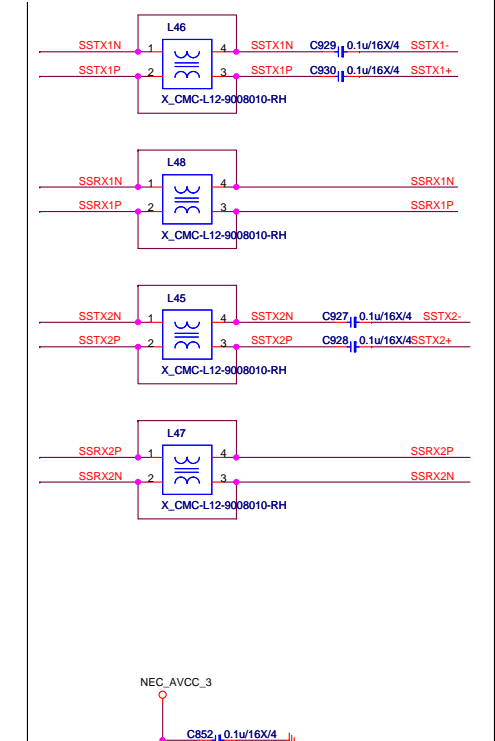
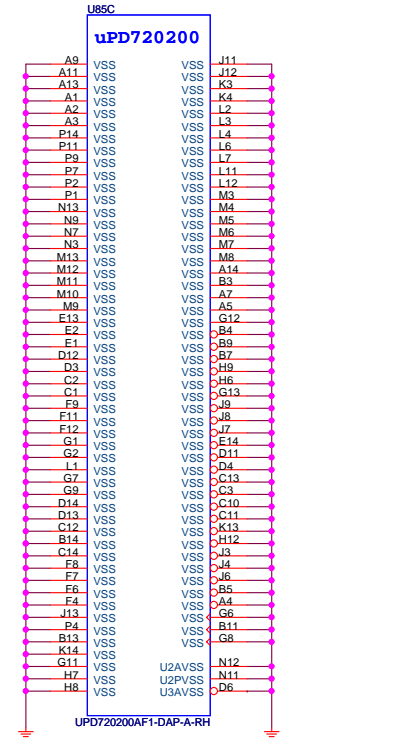
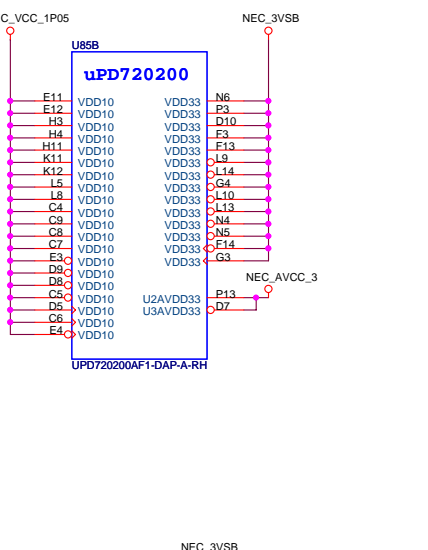
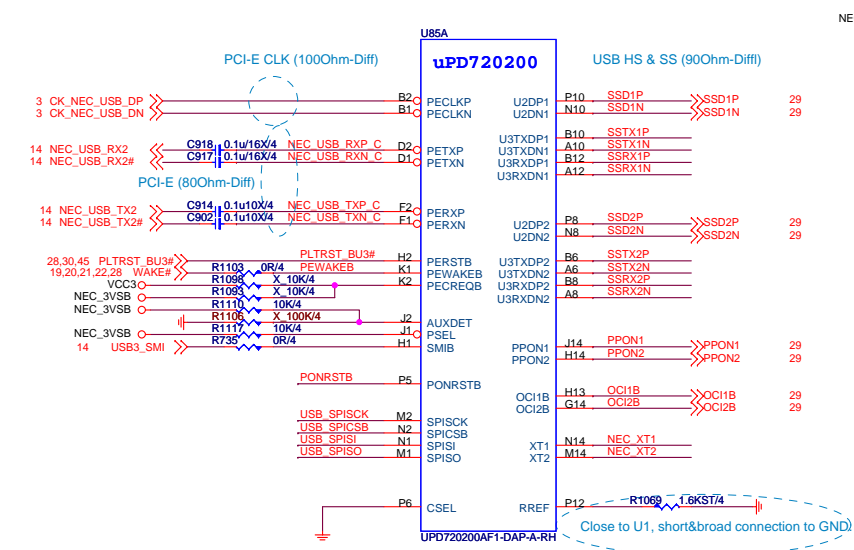
S1	0	0	1
S0	0	1	1
Mode	AUTO	A	Y



A type
 2.70V< D+ <3.1 V
 1.85V< D- < 2.1V
 For i-Pad / i-Phone 4G charges current up to 1.6A.

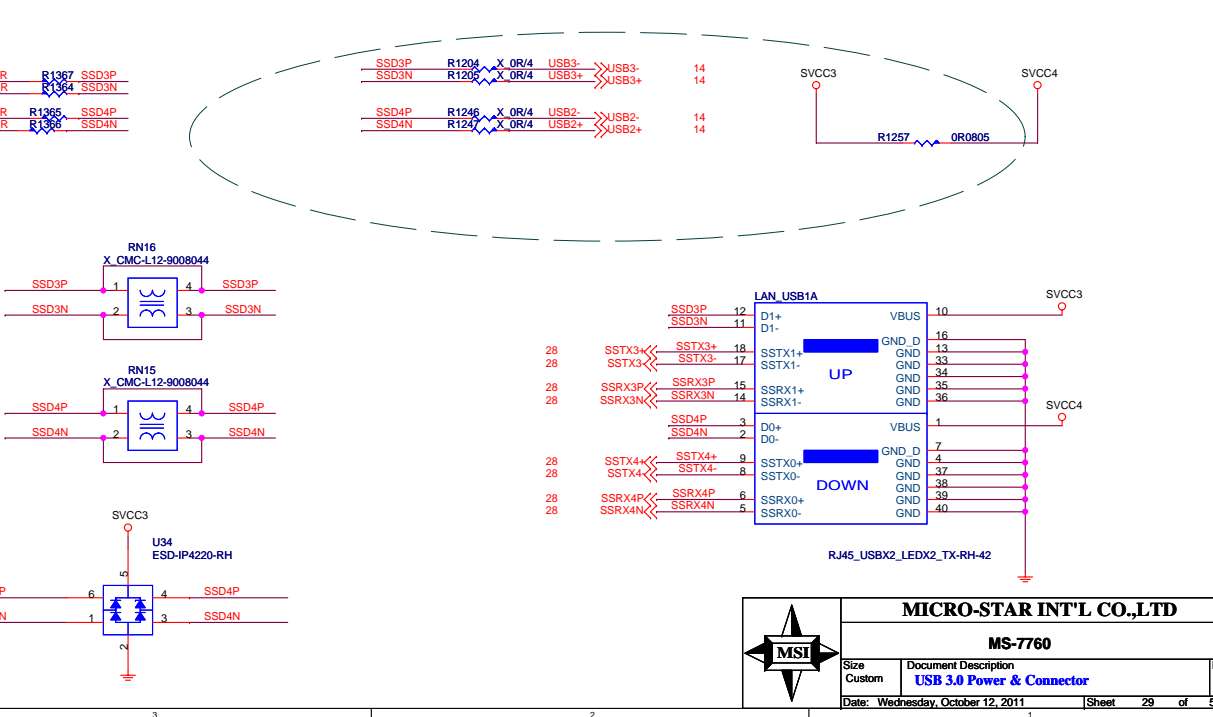
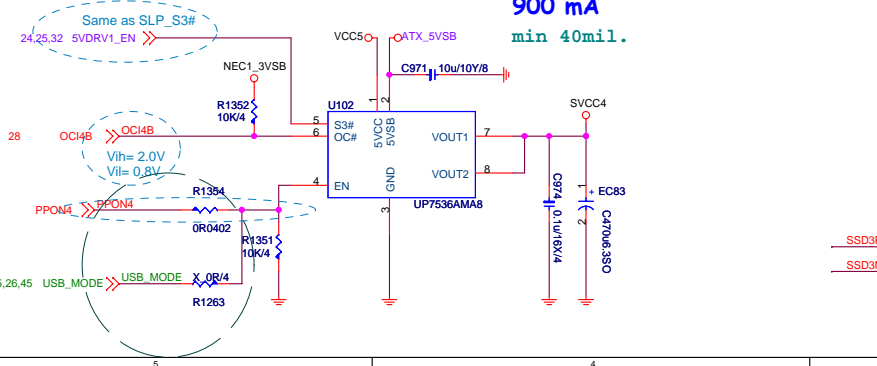
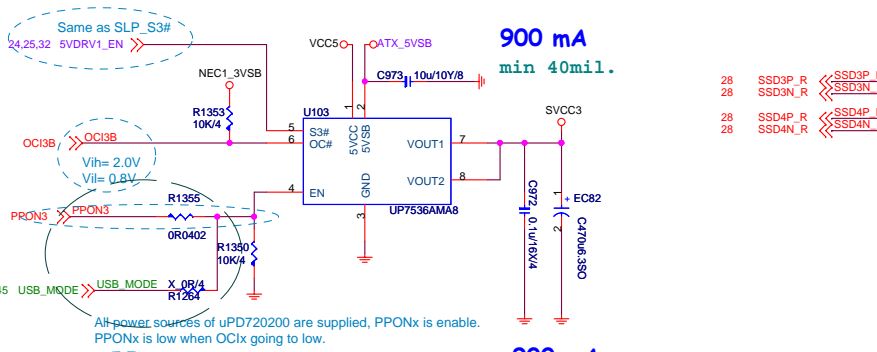
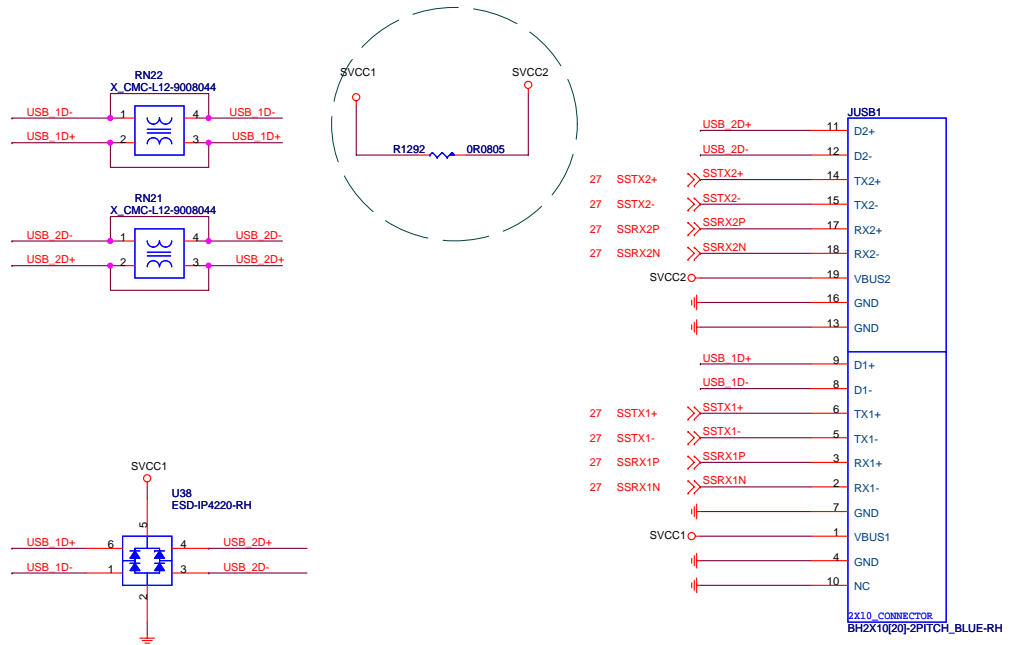
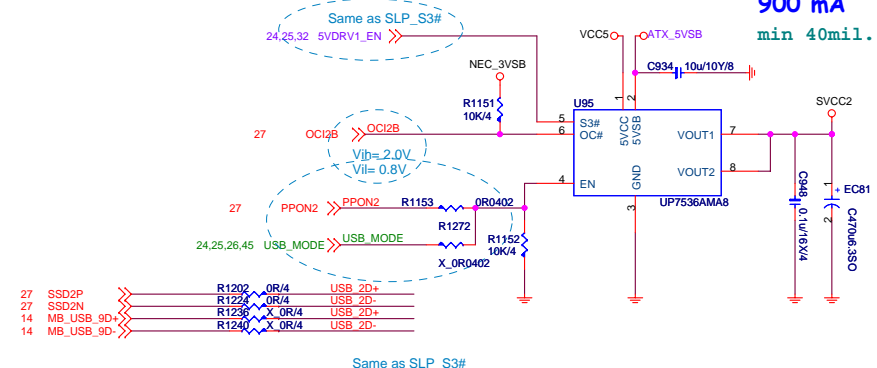
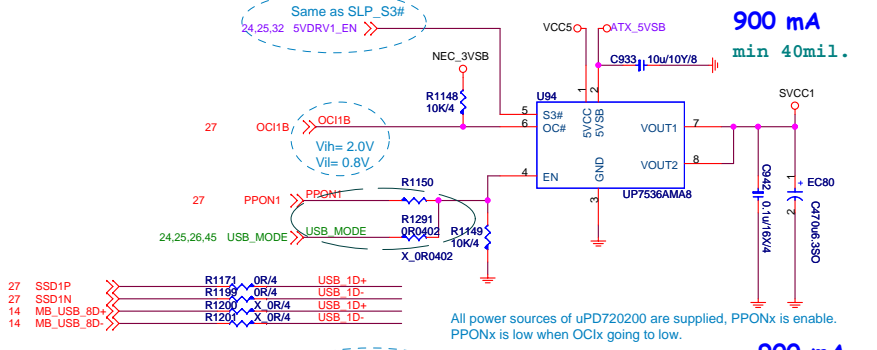


MICRO-STAR INT'L CO.,LTD		
MS-7760		
Size Custom	Document Description Charge Port 0/1	Rev 1.1
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MICRO-STAR INT'L CO.,LTD			
MS-7760			
Size	Document Description		Rev
Custom	UPD720200F1-USB 3.0		1.1
Date:	Wednesday, October 12, 2011	Sheet	27 of 54

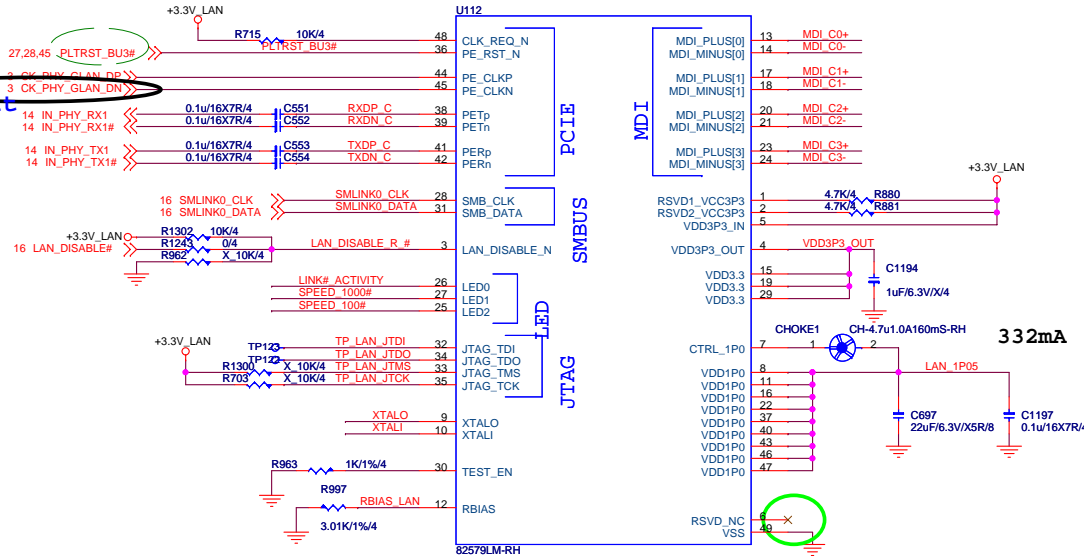
FRONT USB PORT 8,9



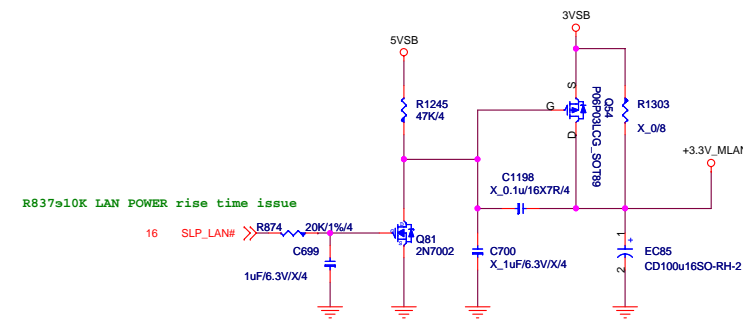
$$V_o = V_{ref}(1+R_2/R_1) + I_{adj} \times R_2$$

If CLK_REQ_N is connected to PCIECLKRQ[1:2]#, the CLK_REQ_N pull-up resistor should be connected to +V3.3s

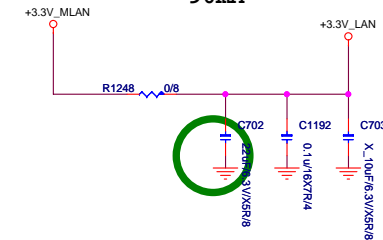
need check it



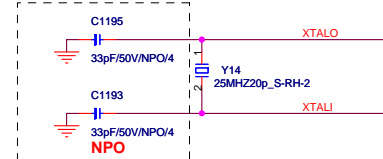
+3.3V LAN



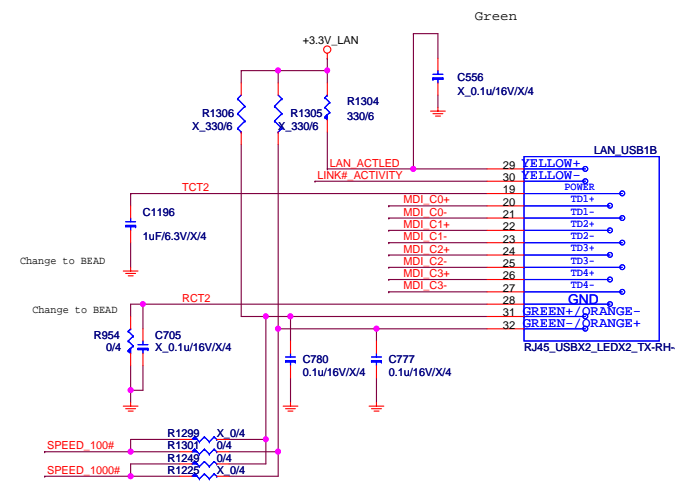
90mA



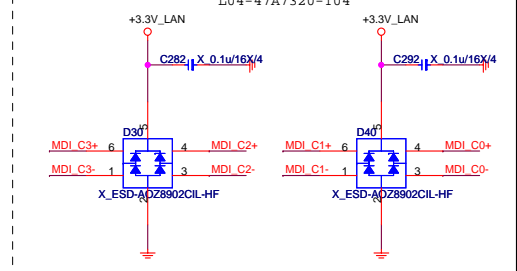
Note: These caps closed to PHY



LAN Connector



CHOKE (> 0.6A) AVLV:
 L04-22A7470-T04
 *L04-47A7340-T04
 L04-47A7330-T04
 L04-47A7320-T04



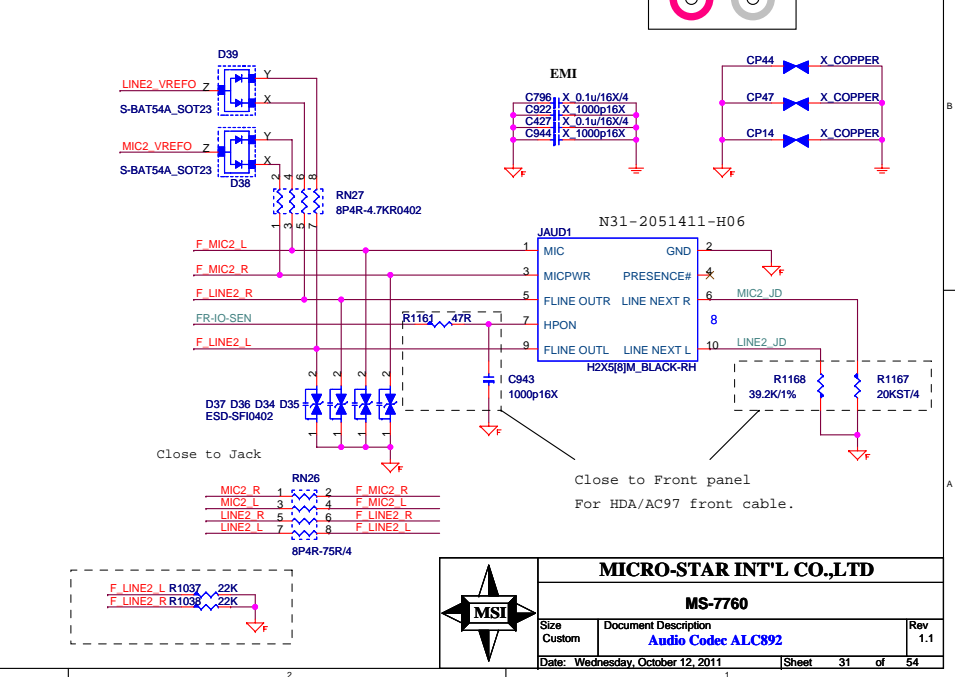
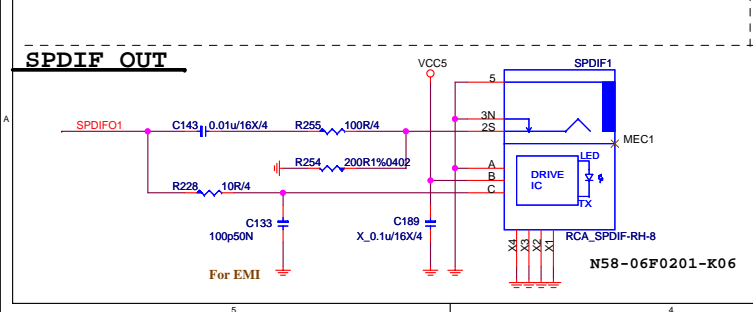
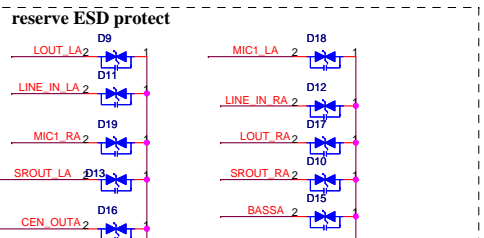
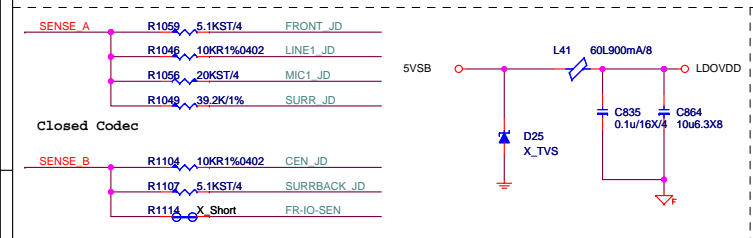
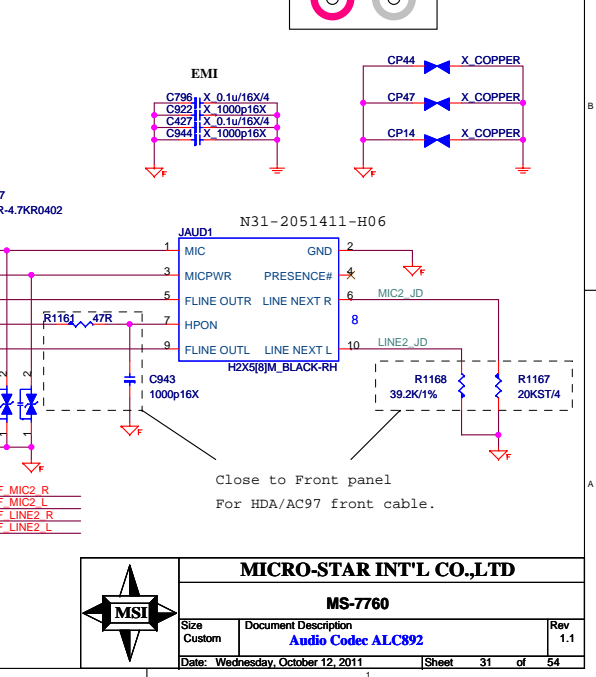
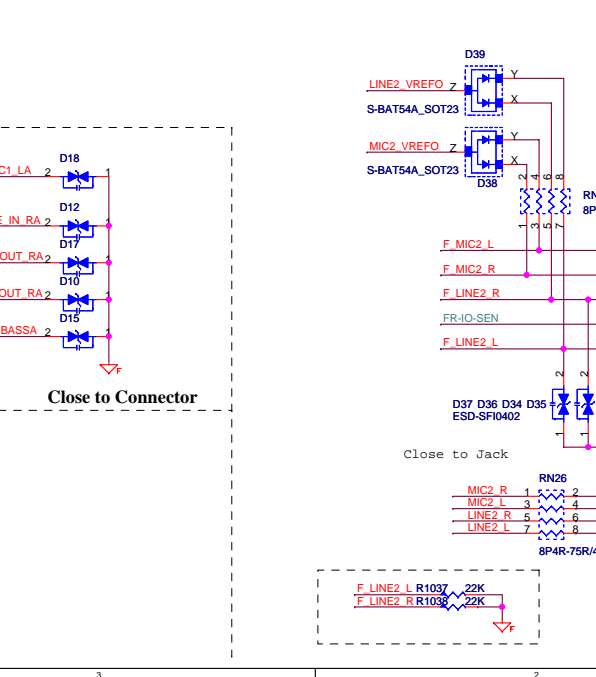
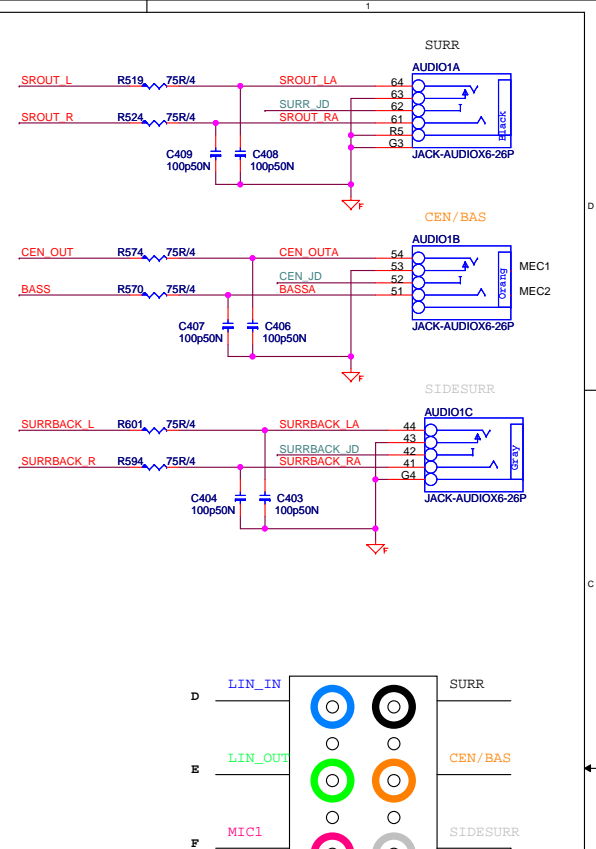
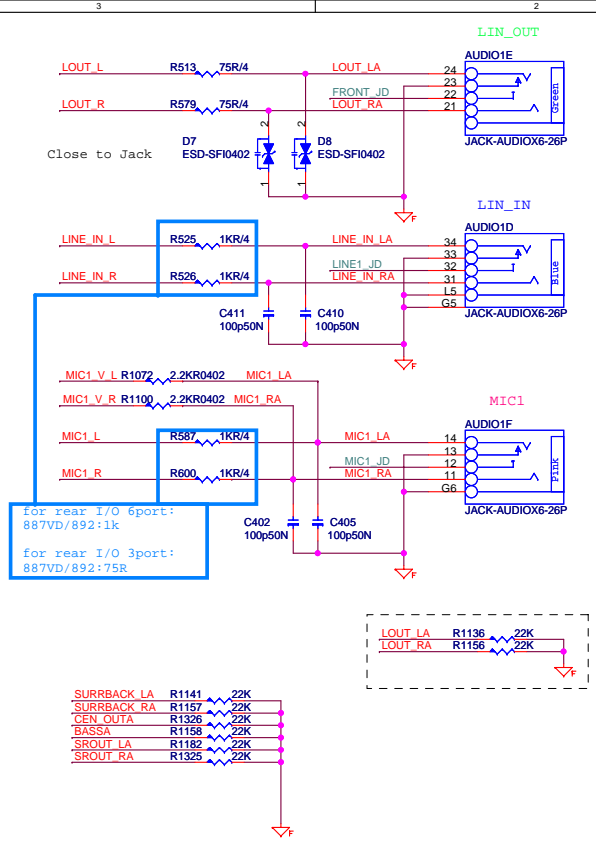
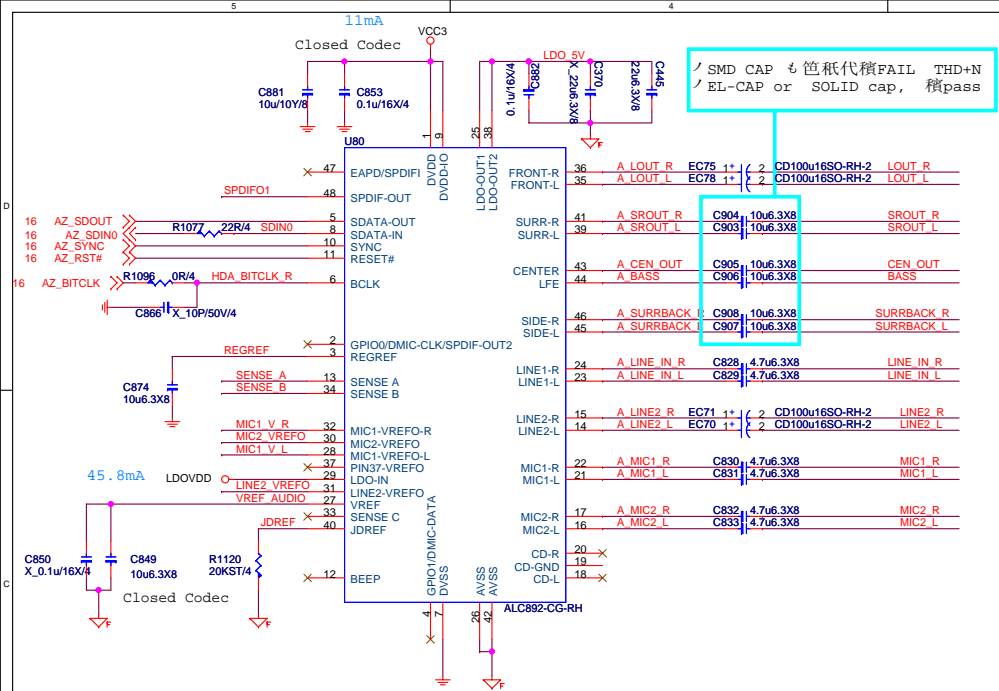
close to Connector close to Connector

JFM38U1K-B301-4*		
JFM38U1J-B301-4*		
JFM38U1H-B301-4*		
JFM38U1G-B301-4*		
JFM38U1F-B301-4*		
JFM38U1B-B301-4*		
JFM38U1A-B301-4*		
JFM38U14-B301-4*		
JFM38U13-B301-4*		
JFM38U12-B301-4*		
JFM38U11-B301-4*		
JFM38U10-B301-4*	NONE	NONE
PART NO.	LED1	LED2

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MS-7760

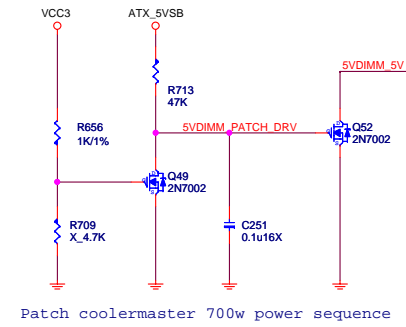
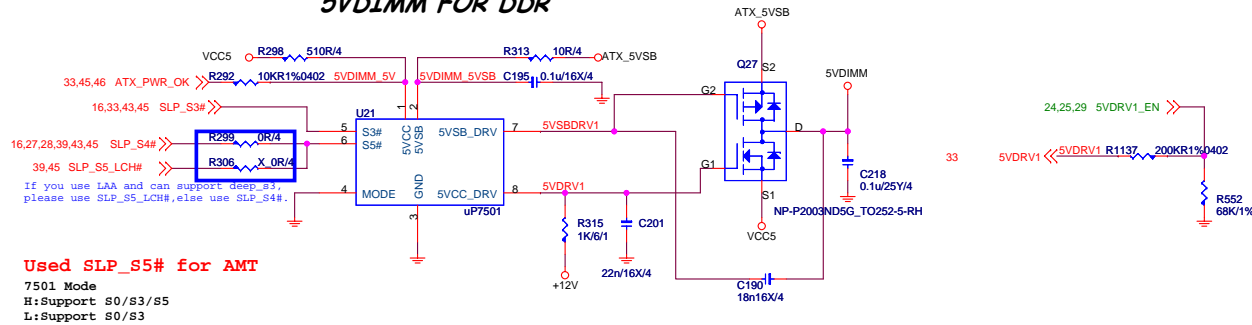
Size	Document Description	Rev
Custom	LAN-RTL8111E-1	1.1
Date: Wednesday, October 12, 2011	Sheet 30 of 54	



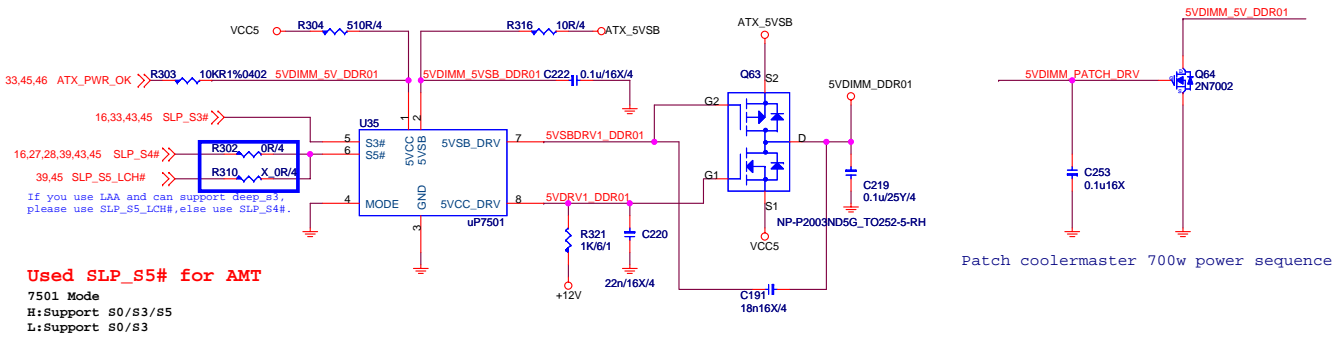
MICRO-STAR INT'L CO., LTD
MS-7760
Audio Codec ALC892

Size	Document Description	Rev
Custom	Audio Codec ALC892	1.1
Date: Wednesday, October 12, 2011	Sheet 31 of 54	

5VDIMM FOR DDR



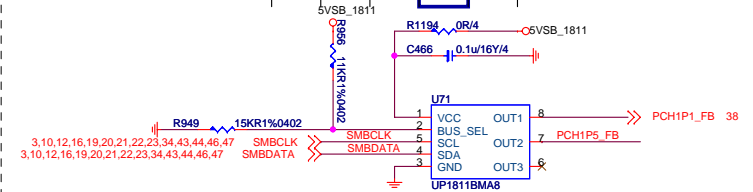
5VDIMM FOR DDR 01



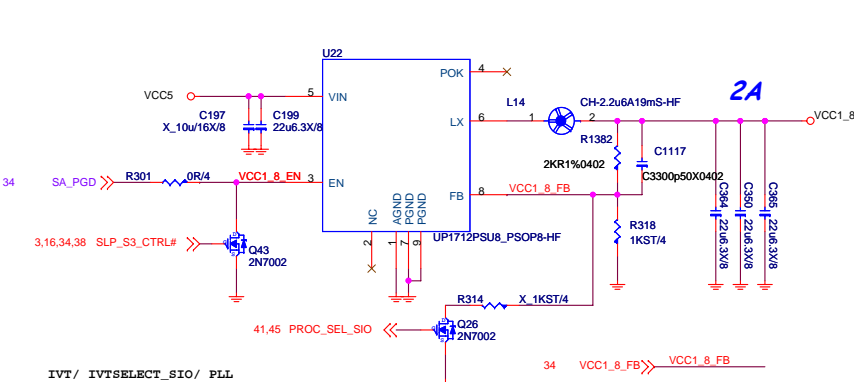
UPI VOLTAGE CONSOLE

0x24:RH=1.1K,RL=15K

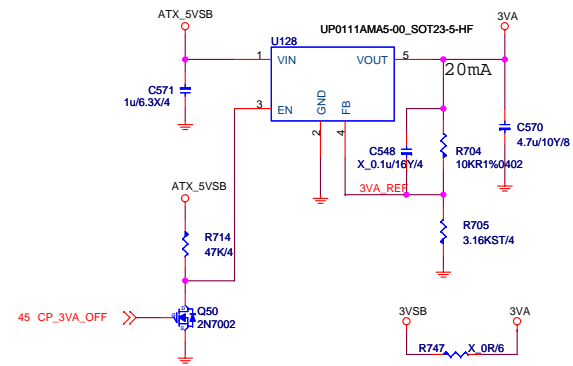
ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (Kohm)	OPEN	3.9	3	2.2	1.3	10
RL (Kohm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%



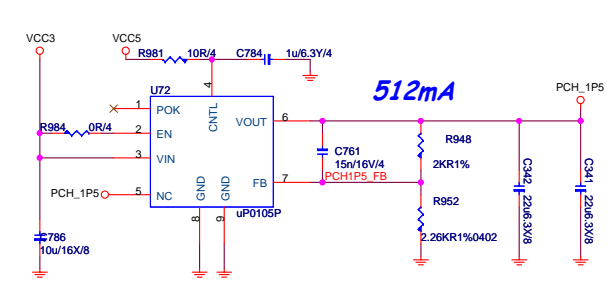
CPU_1.8



3VA



PCH1.5

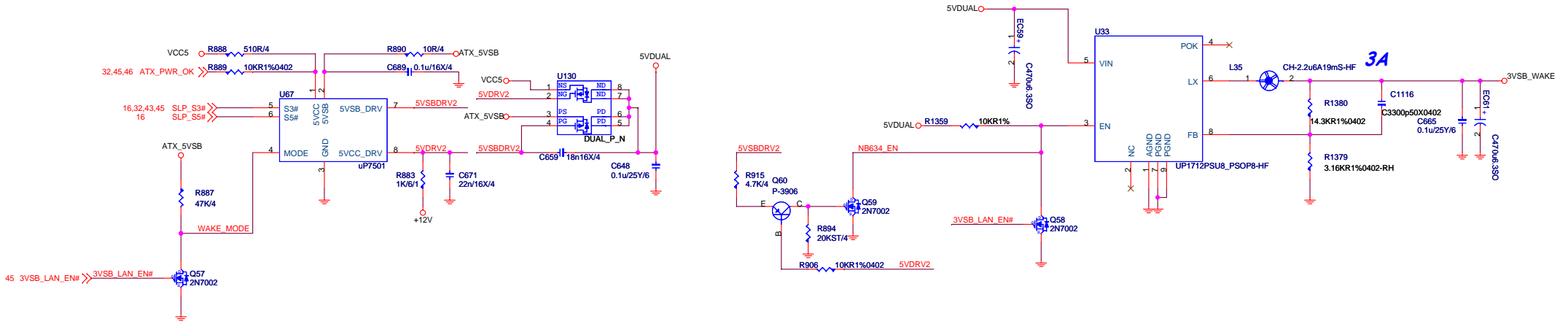


MICRO-STAR INT'L CO.,LTD

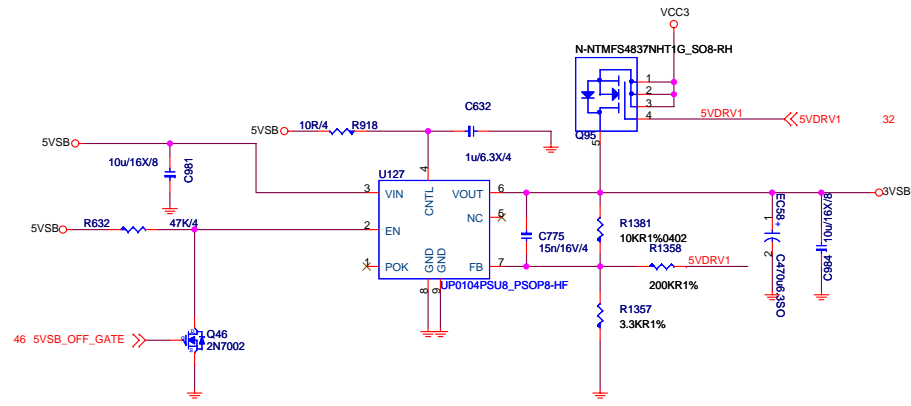
MS-7760

Size	Document Description	Rev
Custom	ACPI controller UPI	1.1
Date: Wednesday, October 12, 2011		Sheet 32 of 54

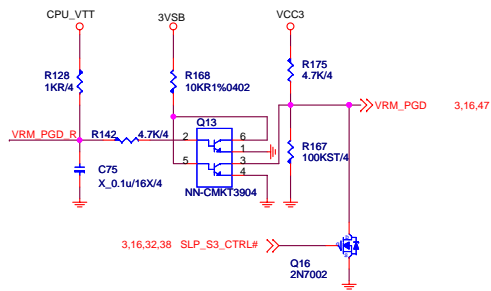
3VSB_WAKE



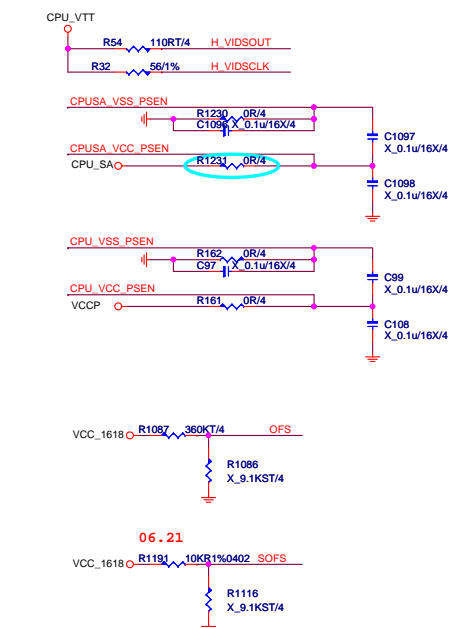
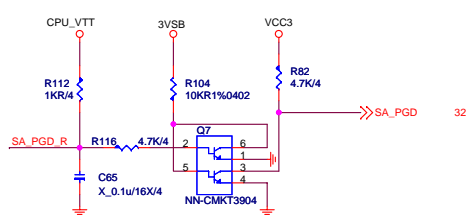
3VSB



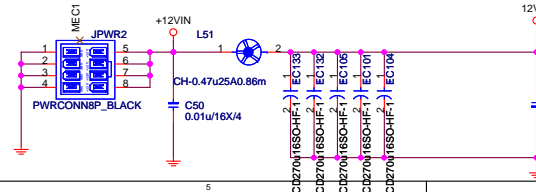
VRMPWRGD LEVEL SHIFT



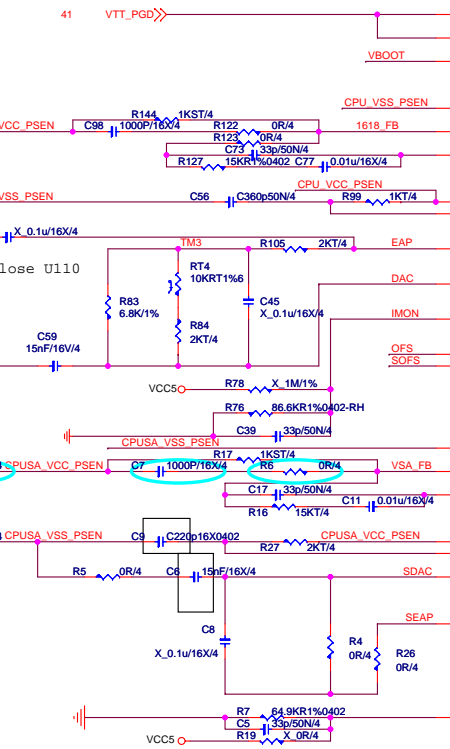
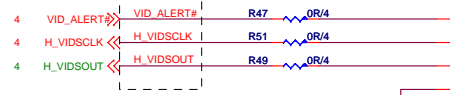
SAPGD LEVEL SHIFT



$5000\text{mA} * 4 * 1 = 20\text{A} > 13.7\text{A} (7.68)$



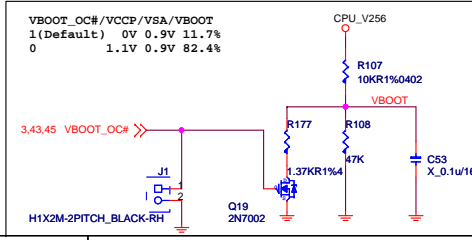
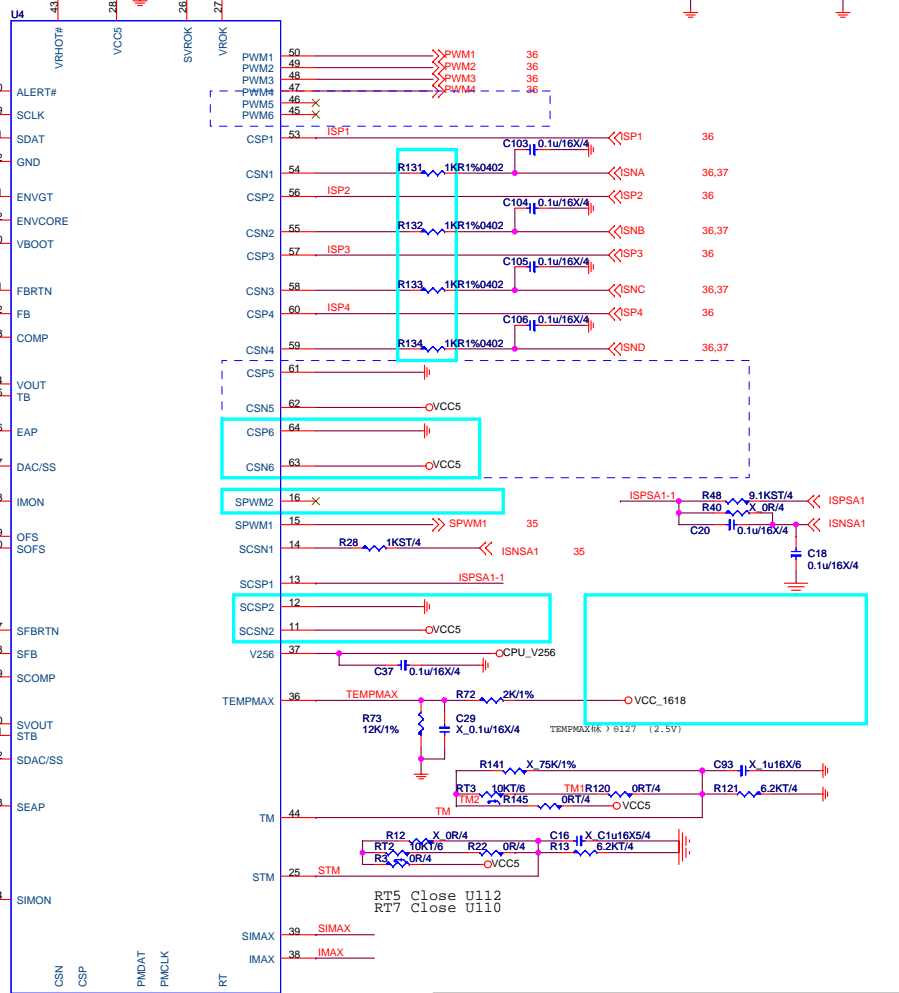
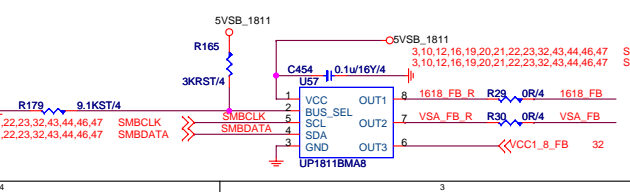
3000mil < L < 6000mil
4mil / 20mil
55 ohm Impedence
must be Referenced GND



UPI VOLTAGE CONSOLE

0x22: RH=3K, RL=9.1K

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

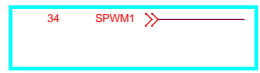
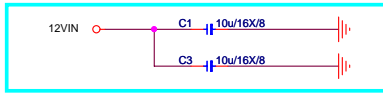
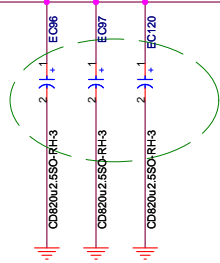
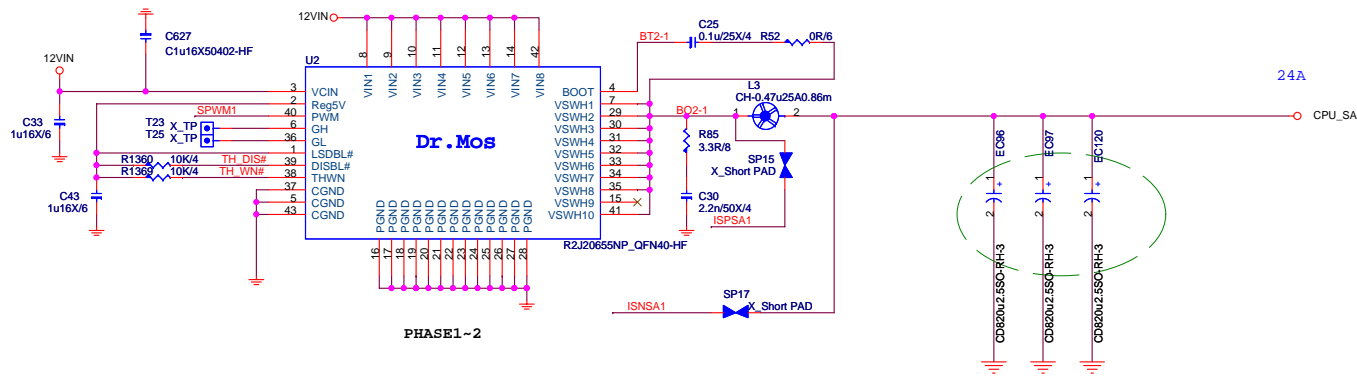


MICRO-STAR INT'L CO.,LTD

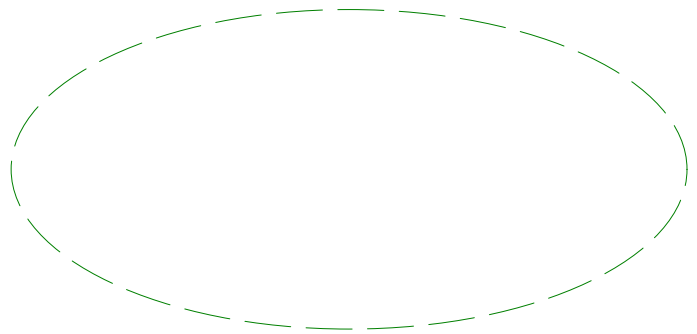
MS-7760

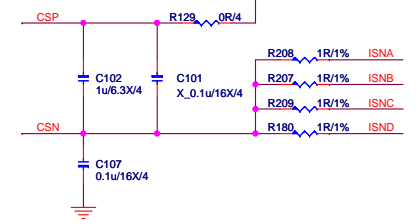
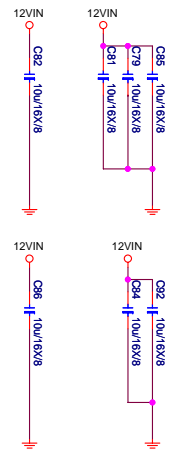
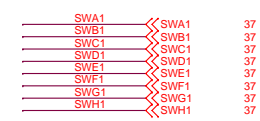
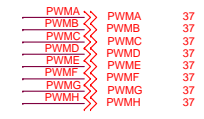
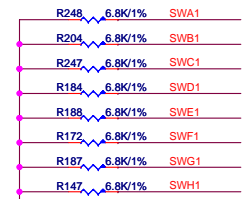
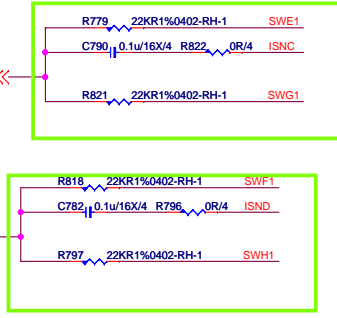
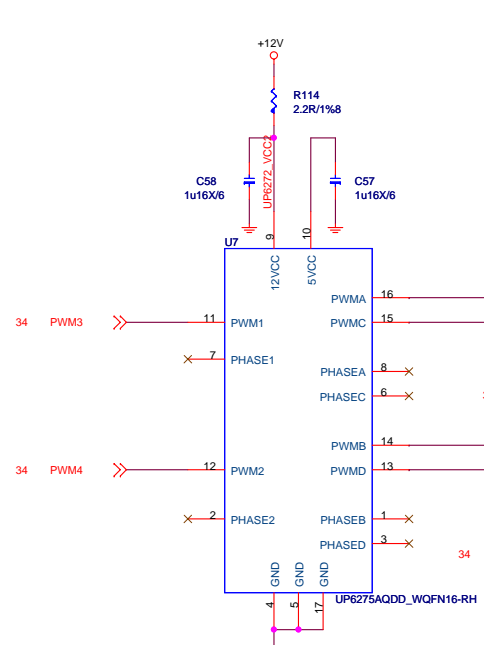
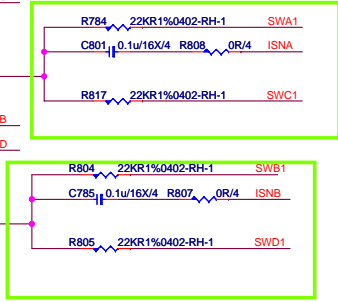
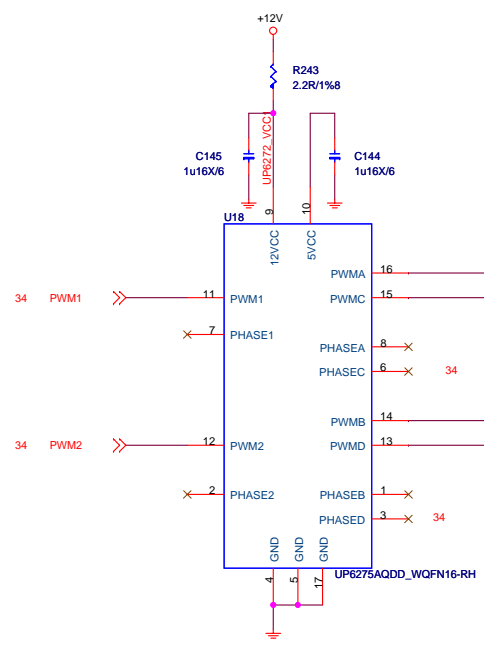
Size Custom Document Description
VRD12 - UPI1618

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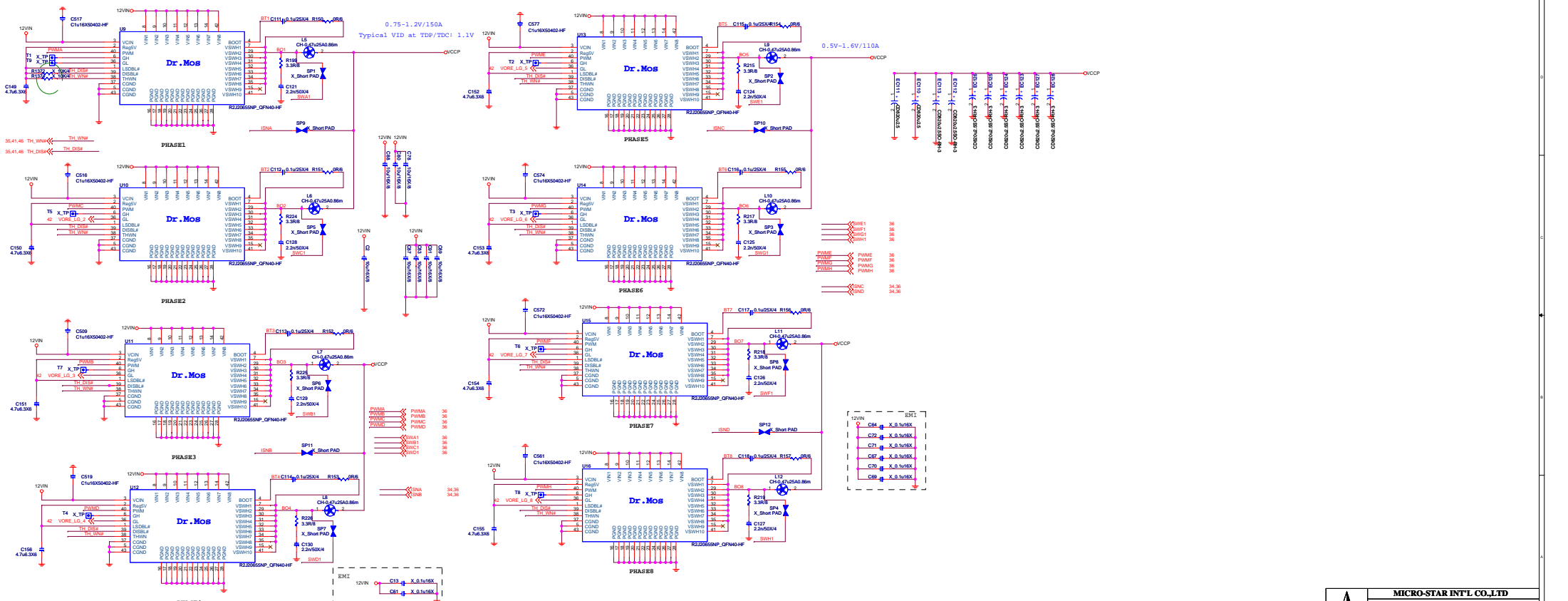


37,41,46 TH_WN# << TH_WN#
 37,41,46 TH_DIS# << TH_DIS#

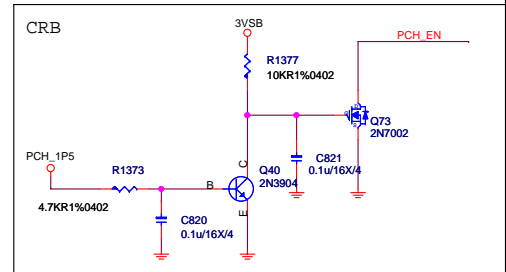
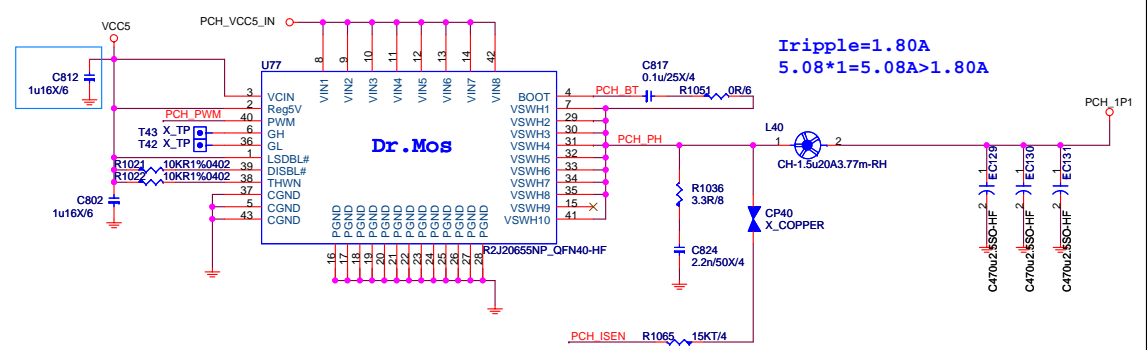
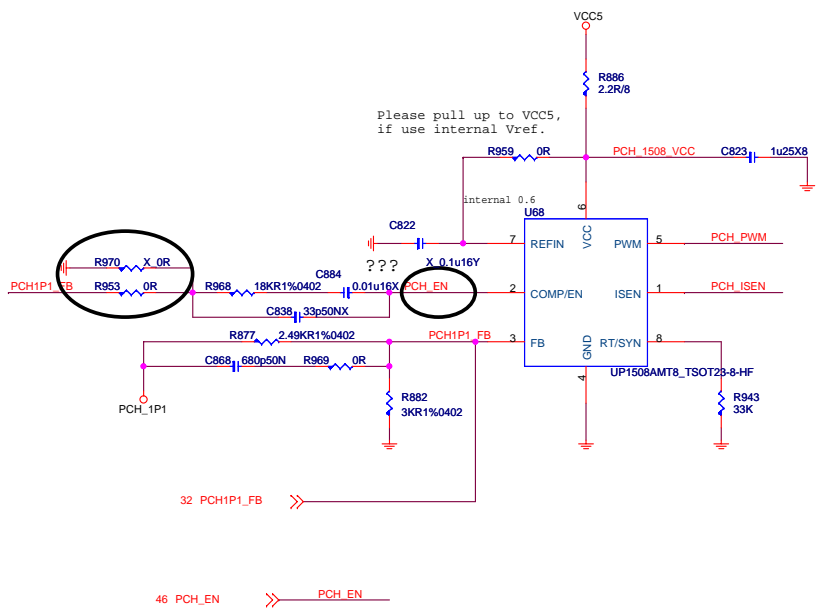




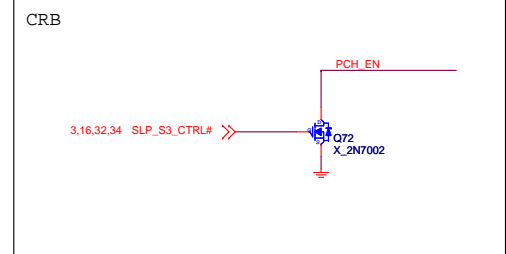
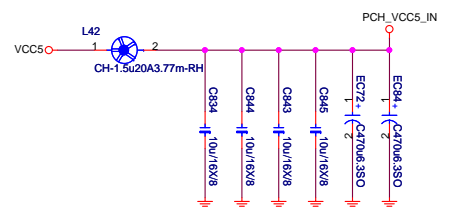
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MS-7760		
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PCH Core 17.2A

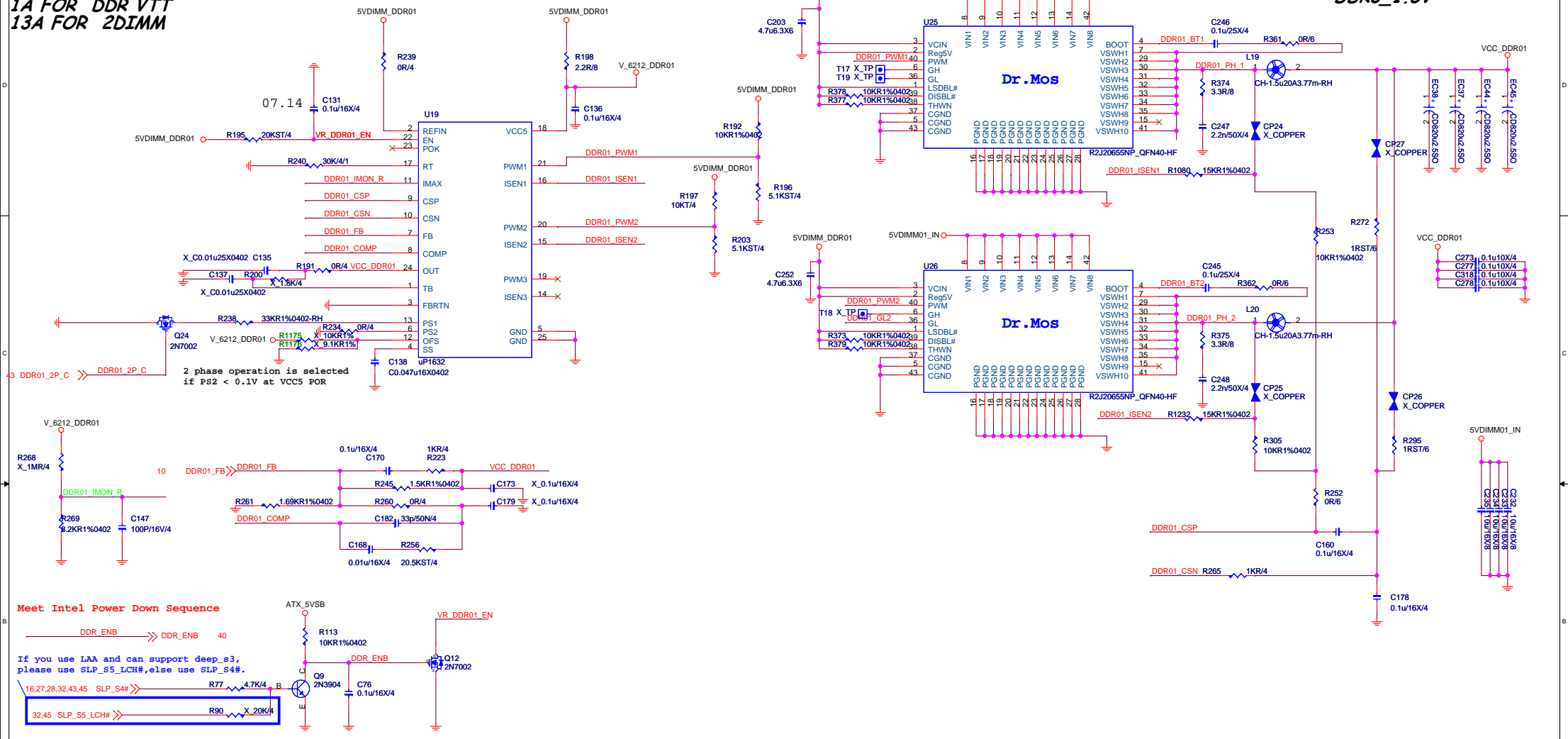


Tripple = 6.2A
5.7 * 2 = 11.4A > 6.2A

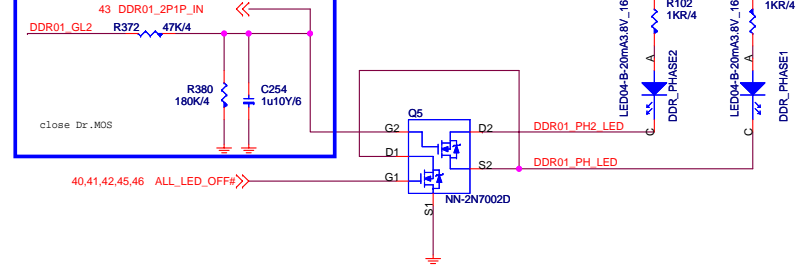


**DDR3 1.5V 20A
3.3A FOR CPU
1A FOR DDR VTT
13A FOR 2DIMM**

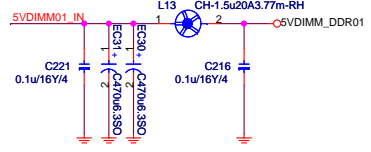
DDR3_1.5V 20A



LED北 結隔

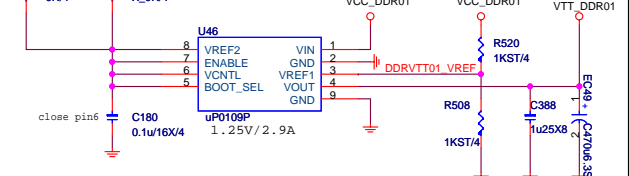


**Tripple=4.25A
4.7*2*1=9.4A>4.25A**



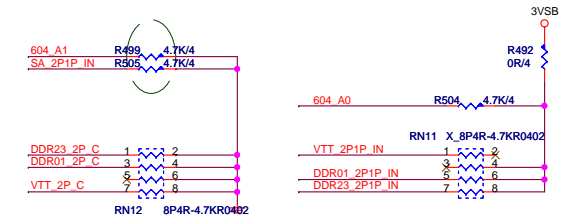
DDR VTT Power

To CPU Copper trace width > 250mils, Fill island behind DIMM > 400mils · 0.5A*2=1A



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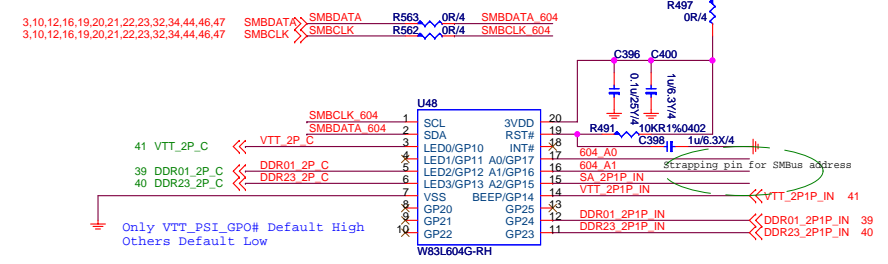
GPIO Controller - B LED / VTT / PHASE6



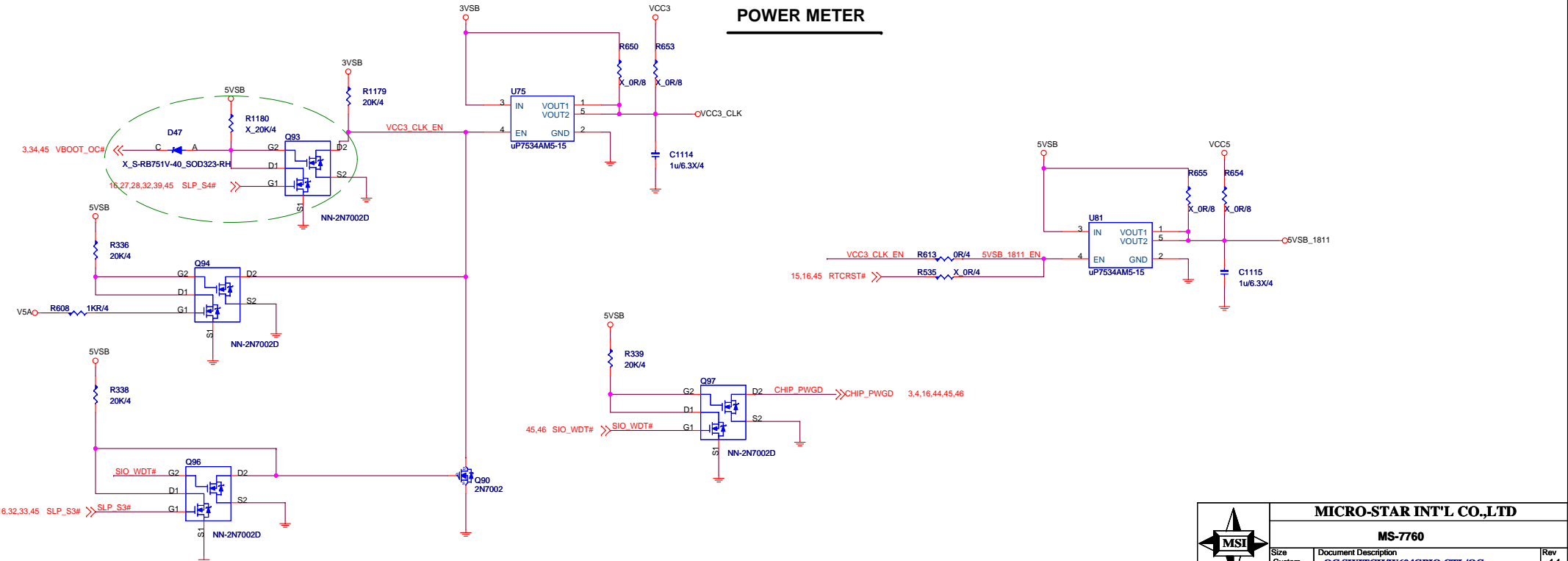
```

Programming
Default GPI ==>GPO(O/D)==>GPO(O)==>GPO(O)
0          0          0          1
    
```

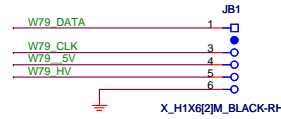
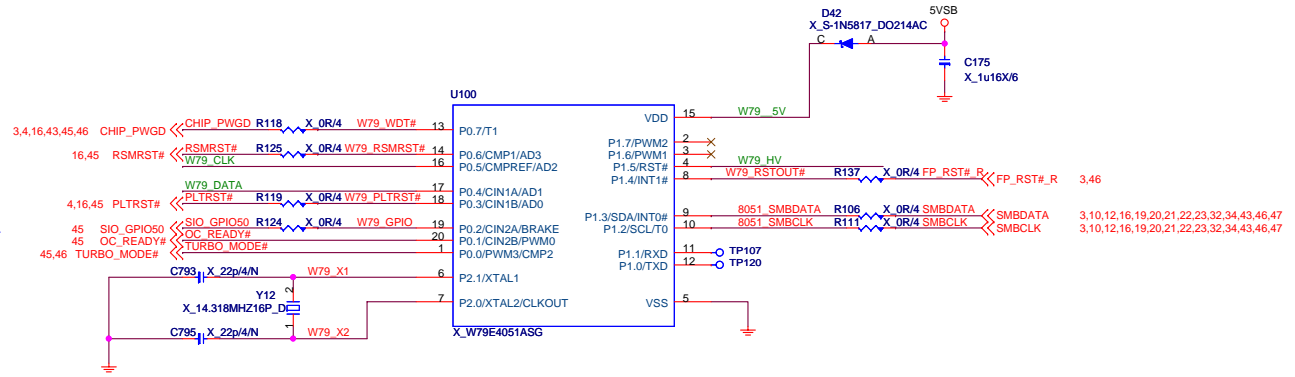
SMBus Address 0X32

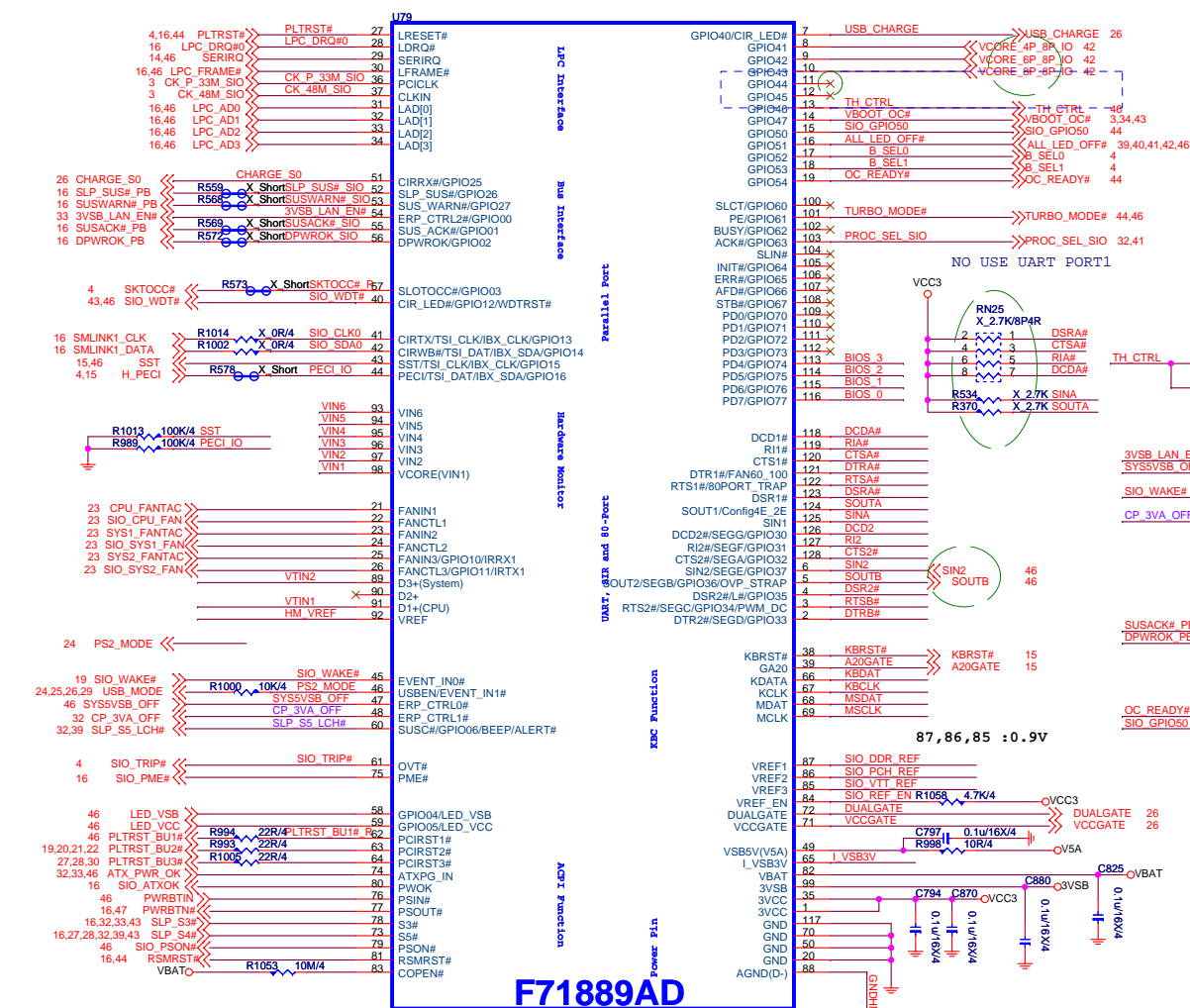


POWER METER

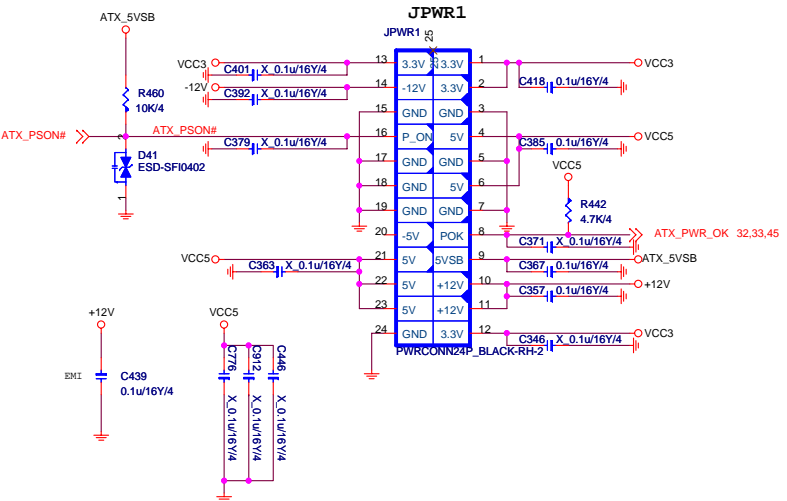


out for Full reset, can pull up to 3V
RSMRST# for 8051 refer to read GPIO state
ICP Programmer
ICP Programmer
PLTRST# is a power on event for 8051
Reserved, can pull to 3V
BIOS inform to 8051 the OC ready, can pull up to 3V
OC Button, can pull up to 3V

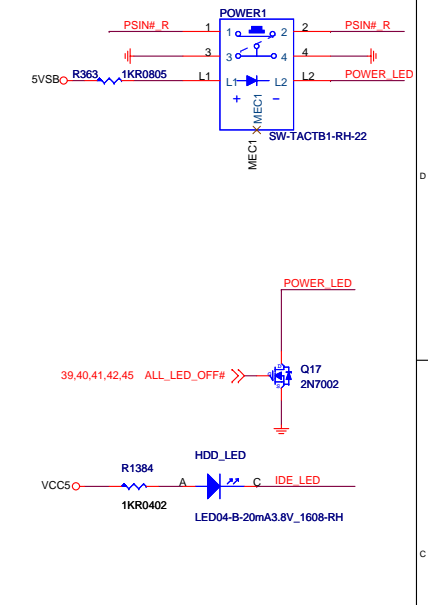
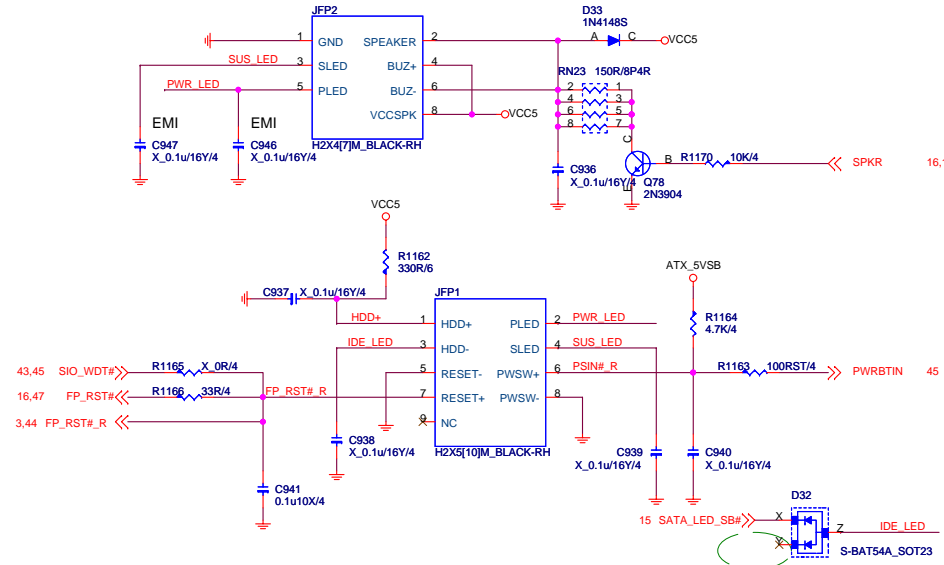




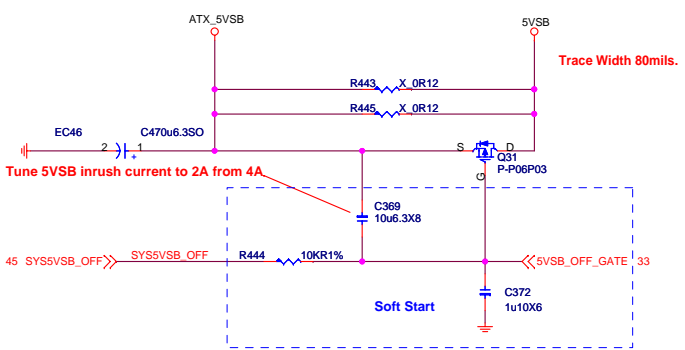
ATX POWER CONNECTOR



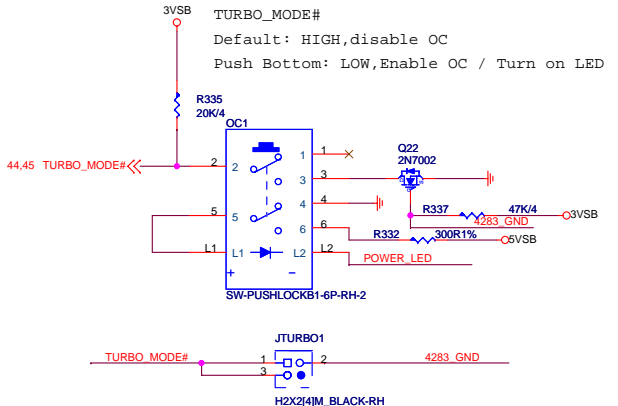
FRONT PANNEL



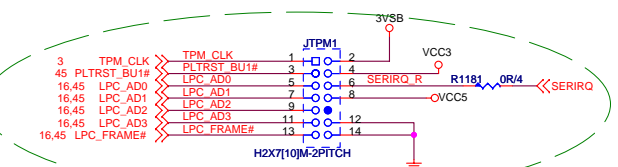
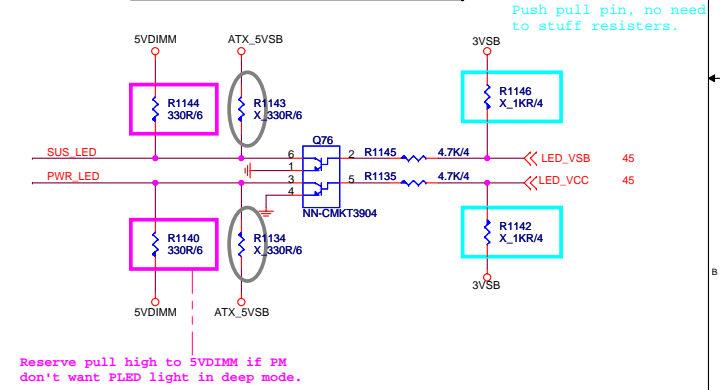
5VSB Power Switch



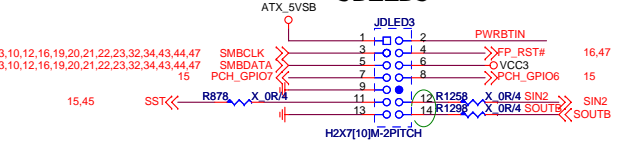
Turbo Button



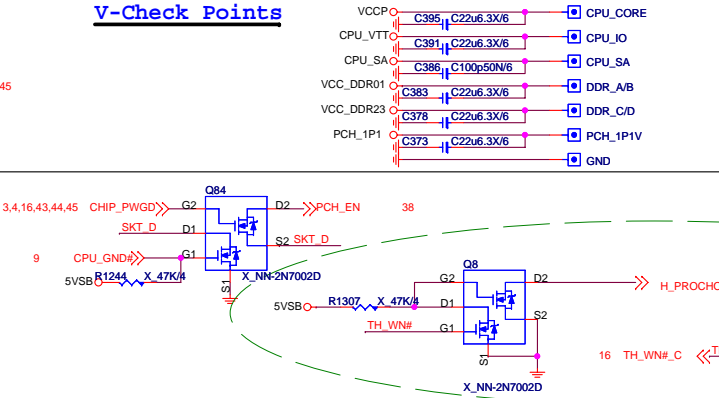
LED (for Fintek 71889)



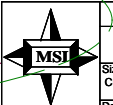
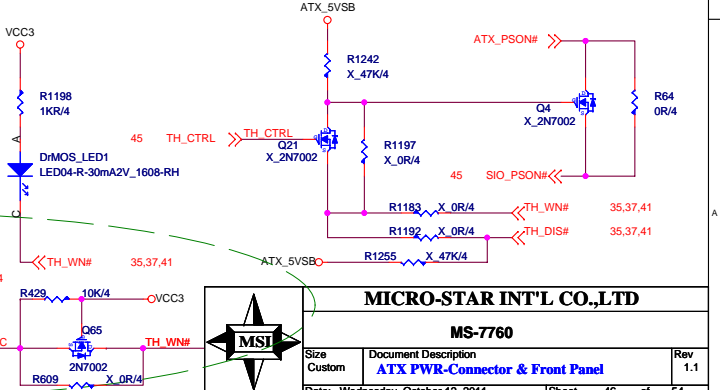
JDLED3



V-Check Points

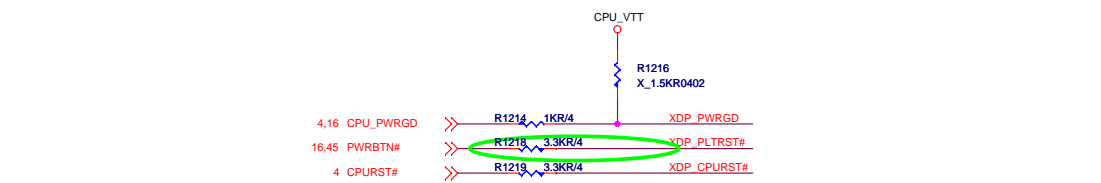
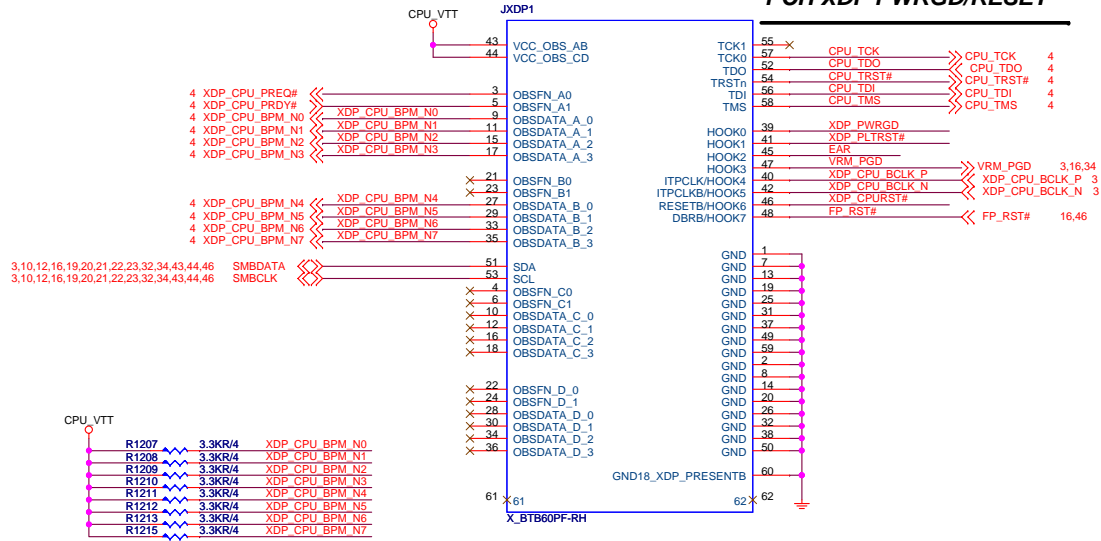


THERMAL SHUTDOWN

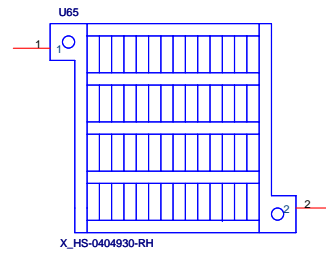
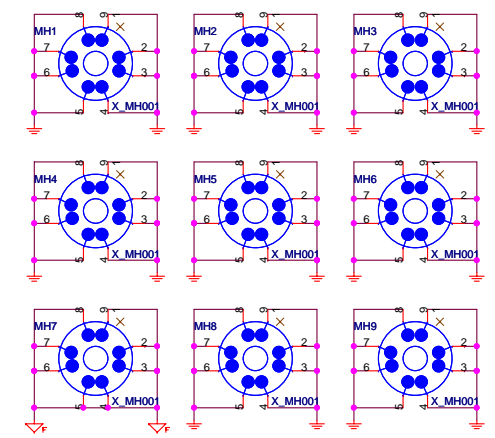


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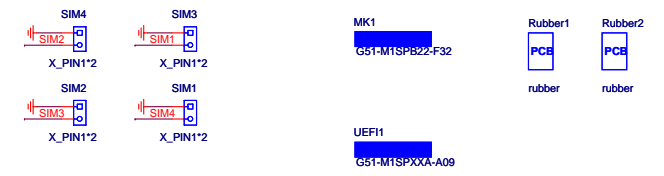
PCH XDP PWRGD/RESET



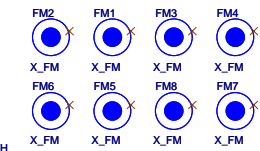
Mounting Holes



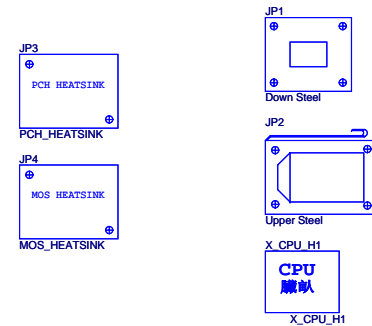
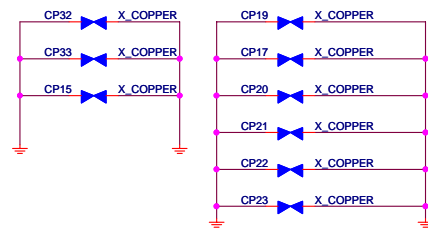
Simulation



Optical Fiducial Marks-120



Optical Fiducial Marks-100



MSI		
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